Differential Power Processing Submodule Integrated Converters for Photovoltaic Power Systems

by

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Date _____

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Choi, Beomseok (Ph.D., Electrical Engineering)

Differential Power Processing Submodule Integrated Converters for Photovoltaic Power Systems

Thesis directed by Prof. Dragan Maksimović

System efficiency of conventional photovoltaic (PV) systems is adversely affected by mismatches among series connected cells, submodules, and modules. Module-level power converters, often referred to as dc optimizers, mitigate mismatch related losses by performing maximum power point tracking (MPPT) locally, at the PV module level. However, dc optimizers must process all PV power and in the process they introduce insertion losses even when there are no mismatches. Differential power processing (DPP) architectures mitigate mismatch-related losses while processing only a fraction of the PV system rated power, and without insertion losses. This thesis is focused on the design, implementation and evaluation of submodule integrated converters (subMICs) in the isolated-port DPP architecture. Using a simple voltage balancing approach where voltage reference is set by the shared isolated port, the subMICs can be controlled autonomously in a distributed manner, without the need for a central controller or communication among units. A custom CMOS controller integrated circuit is developed, which demonstrates voltage-balancing control, power limiting, and protection features on prototype subMICs based on bidirectional flyback converters. A system prototype, including three subMICs, is placed in the junction box of a standard 72-cell PV module, replacing conventional bypass diodes. Performance of the subMIC-enhanced PV module is evaluated through laboratory and outdoor field experiments. Experimental results show greater than 99% module-level efficiency under 25% mismatch, using subMICs rated at one third of the PV power. A performance/cost analysis is performed to select the optimum subMIC design for a given PV system, resulting in best energy-yield improvements at minimum incremental cost.

Dedication

To all who has given me trust.

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Introduction

With increasing focus on global environmental problems, interest in renewable and sustainable energy sources is increasing. Substantial growth can be observed in deployments of renewable energy sources, especially wind and solar. Power electronics is the technology that enables conversion of energy from these sources into electricity delivered to the ac power grid. Improving energy harvesting efficiency and reducing cost of renewable energy are the key goals in further developments of power electronics technology. In particular, solar photovoltaic (PV) systems are gaining popularity in residential, commercial and utility-scale systems due to the decreasing cost and increasing efficiency. of is gaining popularity as an energy source.

A single PV cell generates a very limited low dc voltage, which is not suitable for direct connection or conversion to the ac power grid. In practice, many PV cells are connected in series to obtain a higher dc voltage. Usually, a number, e.g. 60 or 72, of series connected PV cells are assembled into a PV module. PV modules are then connected in series to obtain even higher dc voltages. A dc-to-ac power electronics inverter is then used to converter dc power to ac power delivered to the ac power grid. The non-linear cell current-voltage (IV) characteristic results in the existence of a maximum power point (MPP). A task of the power electronics inverter is to operate the system at the MPP to maximize energy capture.

Due to the series connected nature of the PV cells, mismatches present in PV systems

degrade energy capture performance. Mismatches occur due to partial shading, temperature gradients across the system, tolerances in cell and module parameter, etc. Severe mismatches due to partial shading may cause reverse biasing of shaded PV cells, and "hot-spot" failures due to overheating. Conventional systems mitigate the problem by placing bypass diodes in parallel with substrings of PV cells within the PV module. In the presence of mismatches, the bypass diodes conduct, shorting out portions of the PV system, which results in reduced dc voltage, reduced output power, and losses in energy capture.

Various power electronics architectures have been investigated to address mismatch-related losses. For example, distributed module-level dc-dc converters, known as dc optimizers can be used to perform maximum power point tracking (MPPT) at a finer granularity, thus mitigating energy capture losses related to mismatches. Dc optimizers, however, process full PV power, and introduce insertion losses, even when there are no mismatches in the system. Differential power processing (DPP) methods have been introduced more recently. In DPP approaches, distributed dc-dc converters can operate the PV modules or submodules at MPP while processing on the mismatch portion of power. Partially rated converters can be smaller and less expensive. Furthermore, there are no insertion losses in DPP architectures. Converters in DPP architectures can be applied at a finer granularity level, such as the submodule level, or even down at the cell level.

This dissertation is focused on the design and optimization of submodule integrated converters (subMICs) in the isolated-port DPP architecture [1–3]. Performance of subMIC prototypes is verified in both laboratory and outdoor experiments. Methods of reducing subMIC costs and selecting the optimal subMIC design for a PV system setup are also presented.

The thesis starts with an introduction, including an overview of typical conventional PV systems and technologies used to improve the PV system energy capture performance. The chapter concludes with a summary of the thesis goals and its organization.

1.1 Photovoltaic (PV) Systems

A typical PV system consists of many PV modules connected in series to obtain high DC voltages sufficient for AC grid connection via a power converter: an inverter. A PV system with an inverter connecting the system to the grid is shown in Figure 1.1.

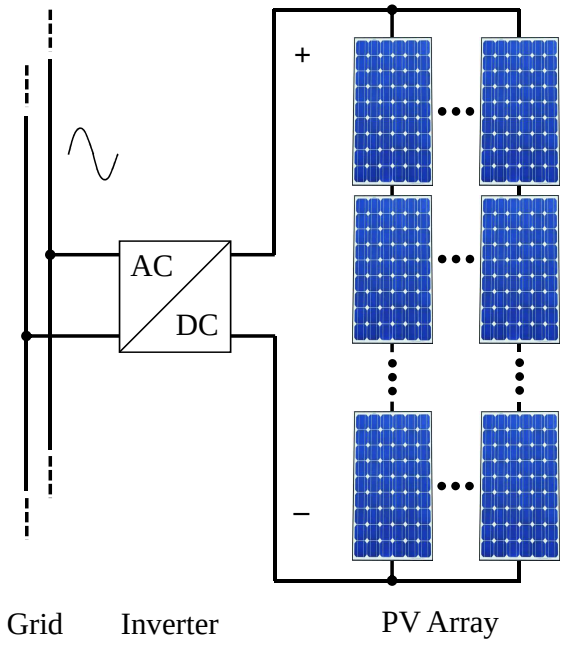


Figure 1.1: A typical PV system setup tied to the grid with an inverter.

The inverter converts the DC power from the PV bus to AC power, It also makes sure the generated power output meets the grid regulation specifications. Also, on the DC bus side, PV voltage is controlled so that the system operates at MPP, hence maximizing the energy capture of the PV system. This is called maximum power point tracking (MPPT). Numerous literatures are available in this topic [4–6]. In order to understand why MPPT is required, the fundamental characteristics of a PV cell must be discussed.

1.1.1 Photovoltaic (PV) Cells

Most PV cells are semiconductor devices which act like a photo-sensitive diode. It can be modeled as in Figure 1.2 as a simple model or a model with parasitics [7].

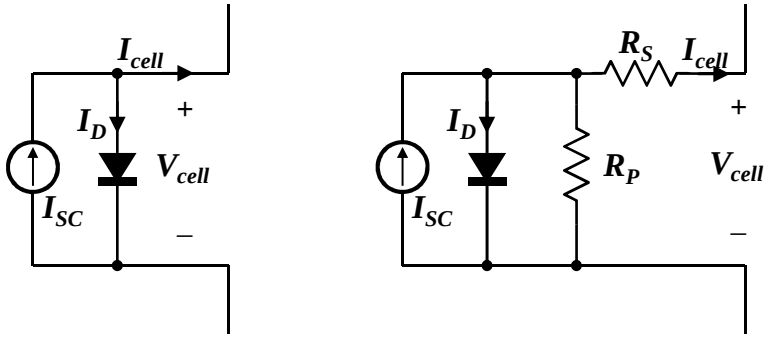


Figure 1.2: PV cell models: simple(left) and with parasitics included (right).

When light radiation hits a cell (also called insolation), current flow (I_{SC}) is generated and partial current (I_D) is flown through a diode. The diode current is dependent on the voltage across the diode. Then the VI characteristic of the PV cell can be found through the following:

$$\begin{aligned} I_{cell} &= I_{SC} - I_D \\ &= I_{SC} - I_0\Big(exp\Big[\frac{V_{cell}}{nV_T}\Big] - 1\Big) \end{aligned} \tag{1.1}$$

If the parasitics associated with the cell (R_S, R_P) are included, then:

$$I_{cell} = I_{SC} - I_0\Big(exp\Big[\frac{V_{cell}}{nV_T}\Big] - 1\Big) - \frac{V_{cell} + I_{cell}R_S}{R_P} \tag{1.2}$$

If the i_{cell} and v_{cell} are plotted for v_{cell}, the characteristic of the PV cell can be seen. Plots of the cells are shown for different insolation levels in Figure 1.3. The plots are called the IV and PV curves, respectively. As insolation increases, power increases. Note that the plot also show reverse breakdown characteristics at $-V_{break}$, which is not modeled in Figure 1.2.

The Y-axis crossing of the IV curve corresponds to I_{SC}, the short circuit current of the cell. I_{SC} scales with insolation. The X-axis crossing is defined as the open circuit

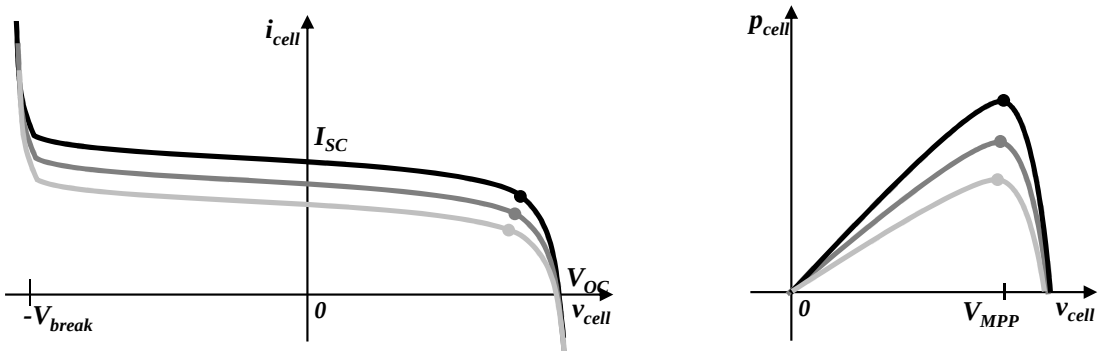


Figure 1.3: The IV curve (left) and PV curve of the first quadrant (right) of a PV cell shown for different insolation.

voltage, V_{OC}. V_{OC} depends strongly on temperature as V_T is a temperature dependent variable. Hence, V_{OC} decreases as temperature rises. Typically, V_{OC} is about 0.6 V for mono-crystalline silicon cells.

The second quadrant of the IV curve suggests that the PV cell can actually dissipate power even when insolation is present. Operating in this region can cause the cell to overheat and damaged in the worst case. Cells operating in this region are known to cause "hotspots" [8, 9] due to the overheating. Therefore, it is critical to maintain positive v_{cell} to prevent operation in this region.

Also, the PV curve in Figure 1.3 shows that a peak power operating point exists. This is called the maximum power point (MPP) at V_{MPP}. It is desired to operate each PV cell at this operating point to maximize energy capture.

1.1.2 Conventional PV Systems

Voltage of a single PV cell does not supply enough voltage for efficient power conversion or utilization. Suitable voltage is obtained by connecting PV cells in series, hence conventional PV modules consists of series connected PV cells. A typical PV module structure is shown in Figure 1.4 with parallel bypass diodes.

Bypass diodes are connected in parallel to each PV substring to mitigate the negative

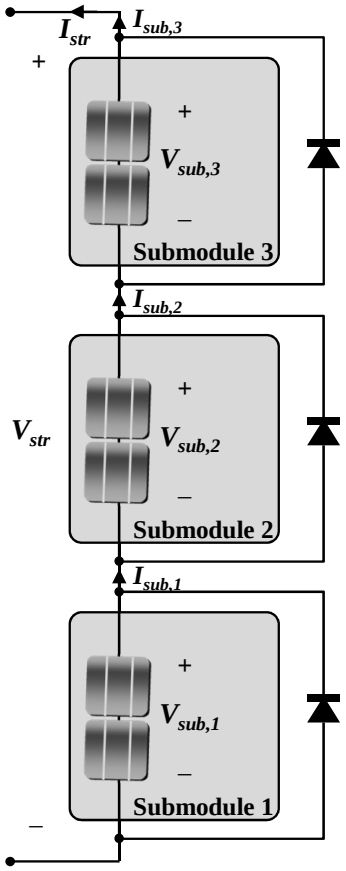


Figure 1.4: Structure of a PV module consisting of multiple substrings with PV cells in series. Typically, substrings have parallel bypass diodes installed.

effects of series connected PV cell. Series connected PV cells operate at a common string current (I_{str}). If mismatch in insolation, temperature, or cell characteristic exists, not all PV cell would operate at MPP. In the worst case, the PV cell could be dissipating power.

One PV cell with low insolation $(cell, 1)$ is shown in the left of Figure 1.5 in a small substring. The IV curve shown on top right of Figure 1.5 shows the issue related to PV cell mismatch. While cell 2 and 3 can operate at MPP, cell 1 is shown to be dissipating power and causing a hotspot. The problem can be mitigated by placing bypass diodes in parallel to the cell. Then, the cell would not be operating at extreme reverse bias. Also, even if the cells are reverse biased, the power dissipation would occur mostly on the bypass diode.

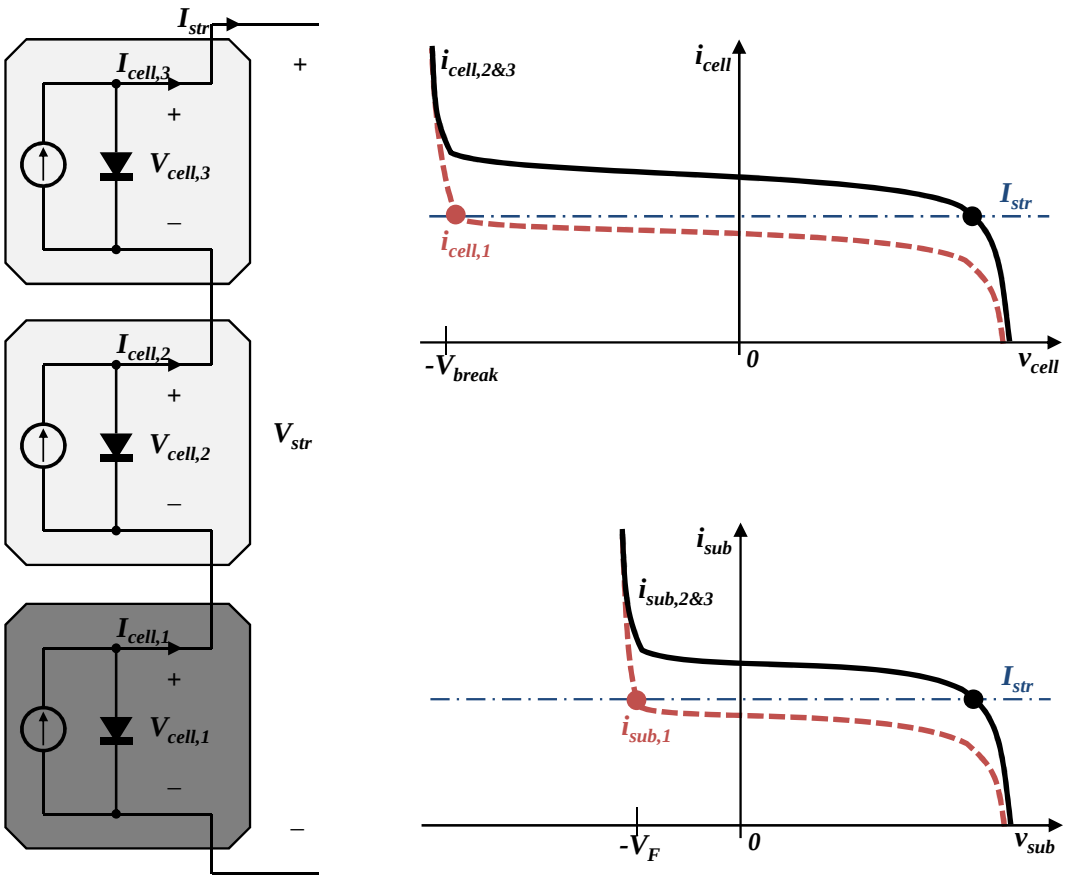


Figure 1.5: A substring of PV cells with mismatch in cell 1(left) with its corresponding IV curve (top right), and the IV curve with bypass diodes at a module level (bottom right).

However, due to the cost, complexity and forward voltage drop of diodes, the bypass diodes are usually placed in parallel at the substring level. The bottom right IV curve of Figure 1.5 shows how the PV module operating points would be at the substring level. Notice that the negative voltage is now clamped to the bypass diode forward voltage drop (V_F).

The conventional system with bypass diodes may prevent severe damage to the PV module while also mitigating severe degradation in energy capture efficiency. However, using bypass diodes are not the best approach and can be improved [10, 11].

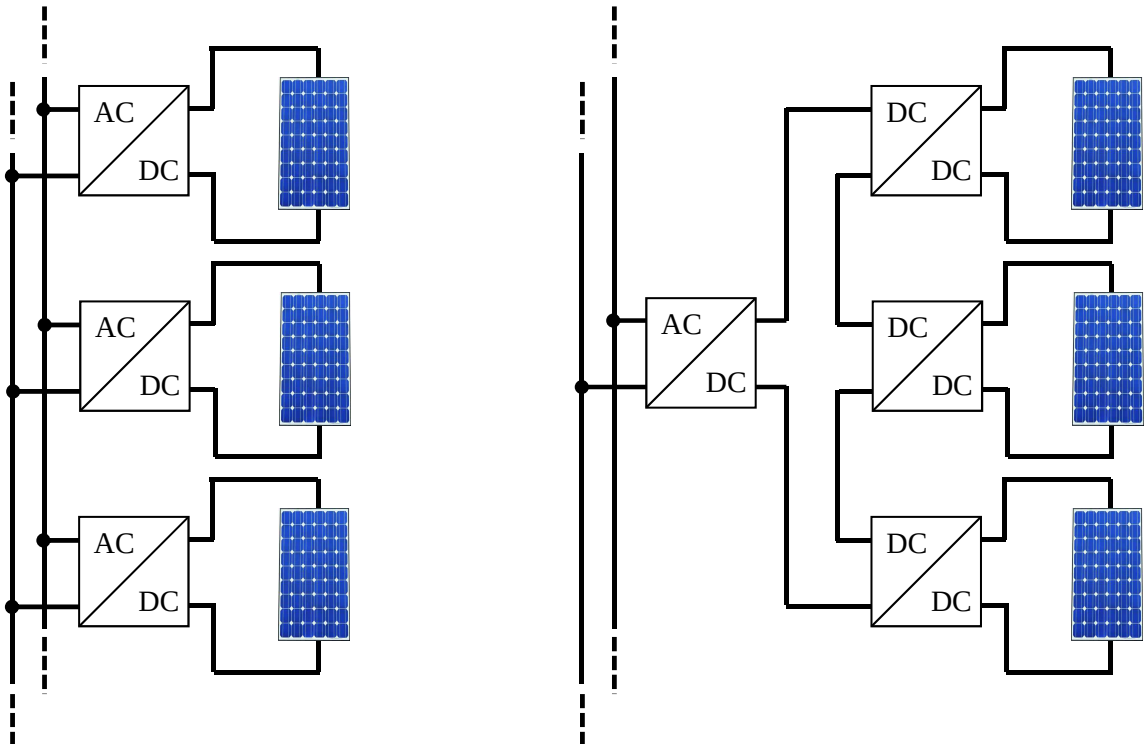


Figure 1.6: Micro inverter PV system (left) and the DC optimizer PV system (right).

1.2 Module Level Power Electronics

In conventional systems as in Figure 1.1, maximum power point tracking (MPPT) is performed at the central inverter to ensure operation at MPP. However, operating the PV bus at MPP does not guarantee that all the PV cells in the system will also operate at MPP. Mismatches in the PV modules and cells are likely to be present,hence not operating at MPP.

MPP at a finer granularity level can improve energy capture. PV Module level power electronics (MLPE) such as micro-inverters [12] and DC optimizers [13, 14] perform MPP at the module level to operate each module at MPP. Also, power processing done at a much finer granularity level are investigated in [15, 16]. The module level MPPT architectures are shown in Figure 1.6. Architectures are discussed assuming module level implementations.

Both micro-inverters and DC optimizers enhance system level energy capture by ensuring MPPT at the modular level. The significant difference between the two architectures is that the micro-inverter does not require a large central inverter. On the other hand, the DC optimizer retains the same grid interfacing inverter and DC bus.

In a micro-inverter system, the power converters usually boosts the PV module voltage directly to the grid voltage. Also, the switches used in the converters would be rated at the grid voltage. Each micro-inverter power rating would be smaller than the conventional central inverter, but the voltage rating would be the same. The efficiency of power processing (via converters) in the system can be expected to be similar to the conventional central inverter case due to the identical voltage rating, but overall energy capture would be relatively better due to finer granularity MPPT.

As for the DC optimizer, the DC-DC converter outputs are connected in series. The sum of the output voltages determines the DC bus voltage to the central inverter. Unlike the micro-inverter, the voltage ratings scale down as more DC optimizers are connected in series. However, this architecture still requires the central inverter.

It is not directly clear which architecture is more cost effective or efficient. However, it can easily be seen that the added converters process all the power of the PV modules (full power processing). Given the efficiencies of the converters, the maximum energy obtainable from the system will have the following relationship:

$$E_{micro-inverter-system} \leq \sum_{i=1}^{N} E_{PVmodule,i} \cdot \eta_{micro-inverter} \tag{1.3}$$

$$E_{DC-optimizer-system} \leq \sum_{i=1}^{N} E_{PVmodule,i} \cdot \eta_{DC-optimizer}\eta_{inverter} \tag{1.4}$$

The full power processing architectures have energy capture efficiency limited by the converter efficiency at all times. More on the actual performances can be found in the previously referred literatures.

1.3 Differential Power Processing (DPP) for PV Systems

The converters of architectures discussed in Section 1.2, process all of the energy captured from the PV modules. Going back to the fundamental problem of series connected PV cells, it can be noted that the problematic issues arise from the common current operating point. When mismatches among series connected cells exist, not all cells can operate at MPP. If the mismatched cells can be operated at different current operating points, all cells could operate at MPP. In order to operate each cell with independent current, the difference in current must be diverted through an auxiliary path as power. This method is commonly called differential power processing (DPP). Figure 1.7 show the simplified operation of the DPP PV system.

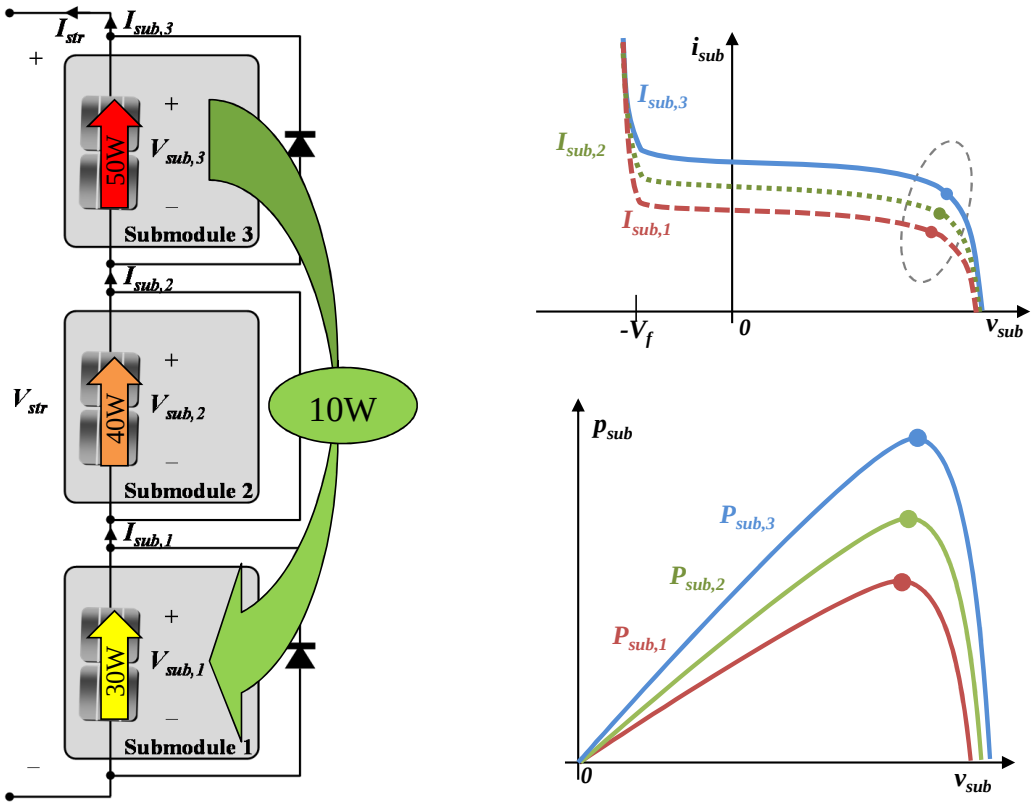


Figure 1.7: Power balancing in a DPP PV system (left) and the corresponding operating points shown(right).

Numerous literature on DPP architectures with various architectures are proposed [1, 17–20]. Among them, few architectures are shown in Figure 1.8: PV-to-PV shuffling [17], isolated PV-to-bus [18], and isolated port PV-to-bus [1]. Substring scale implementation is assumed in the figure.

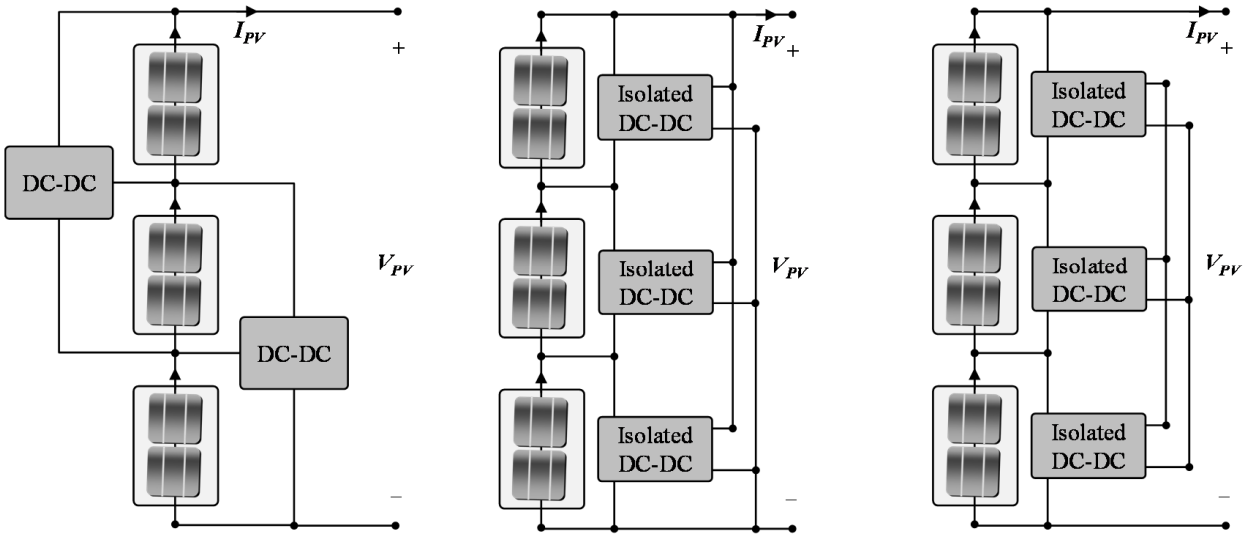


Figure 1.8: Various DPP architectures: PV-to-PV shuffling (left), isolated PV-to-bus (center), and isolated port PV-to-bus (right).

The PV-to-PV shuffling architecture processes the mismatched power between adjacent substrings. However, it can still balance mismatched power for non-adjacent substrings. The architecture requires one less bi-directional converter than the number of substrings in series. In this architecture, the total power processed in the converters varies with the position of the mismatch, even when mismatched power is the same.

The isolated PV-to-bus architecture requires isolated bi-directional converters. While one side of the converter is connected to a dedicated substring, the other side of the converter is connected in parallel to other subMICs and the PV bus. This architecture requires isolated converters. Mismatched power is processed via the added bus. It is used to reroute power in and out from the substrings. If minimal power processing is desired, a central controller

is required to determine the power processing scheme.

The isolated port PV-to-bus architecture is similar to the isolated PV-to-bus architecture, but does not have the auxiliary bus connected to the PV bus. Compared to the isolated PV-to-bus architecture, the minimum power processed can be sub-optimal due to the lack of power flow from the PV bus. However, the isolated bus is no longer required to be at PV bus voltage. The flexible axillary bus voltage allows the use of lower voltage rated devices.

Each architecture has its trade-offs regarding system performance improvement, size, and costs. Analysis in [21] compares the probability of power processed in the converters for a PV system with 10% deviation over 8 PV elements. The compared architectures are the PV-to-PV shuffling and isolated PV-to-bus architectures. Results in the analysis show that most of the power processed by the converters in the isolated architecture are below 15% of the module full power rating. On the other hand, the shuffling architecture processes power over a wide range with mean at 35%.

Viewing the results at a cost and size perspective, the shuffling architecture would likely be small due to the lower voltage rating and no need for isolation. However, the isolated case requires much less power to be processed. Hence, the size and power rating could also be reduced. However, the voltage rating of the converter would be at the PV bus voltage.

The isolated port architecture does not require the isolated bus side voltage to be at the PV bus voltage. If the architecture behaves and performs closely to the isolated PV-to-bus architecture, the converter can be design to be more efficient, smaller, and cheaper.

1.4 Thesis Objectives and Organization

The dissertation goes through the design and realization of submodule integrated converters (subMICs) in the isolated-port differential power processing architecture (DPP). Designing power converters that improve PV system performance is challenged by the improvement versus cost trade-offs. It is critical for the designs to be optimized to perform not

just efficiently, but also cost effectively. The DPP architecture is advantageous in reducing the cost of the converter while requiring less effort in maximizing the efficiency.

In Chapter 2, the isolated port DPP architecture is reviewed. The key advantages of the architecture are discussed, together with the control methods that can be used. The voltage balancing control scheme used in the subMICs is described.

Chapter 3 describes design details of the subMIC prototype. It includes analyzing losses in the power stage for further optimization of design. This includes planar magnetics design to optimize size and reproductivity, and control methods to improve system performance.

Chapter 4 evaluates the prototype design and verifies that it performance. Efficiency and behavior of the converters are evaluated. It also provides a deeper insight into how the controller is implemented on a custom CMOS integrated circuit (IC).

Experiment results for the DPP subMIC system are presented in Chapter 5. Experiments compare the subMIC system with the conventional system under both controlled test environment in the laboratory, and under realistic shading conditions outdoors.

Cost versus performance optimization is presented in Chapter 6. PV system installations can vary from site to site. Also, shading conditions can be very different from system to system. The presented method is developed to find the optimal design of a subMIC for different PV system installations, to maximize energy capture, while minimizing the incremental cost of subMICs.

The last Chapter summarizes the dissertation and presents possible future works.

Chapter 2

Isolated-port DPP Submodule Integrated Converter (subMIC)

This chapter explains the architecture, converter, and control scheme for a submodule level DPP PV system. Many configurations are possible for a DPP architecture, but few specific ones are discussed in this chapter. First, the isolated-port DPP architecture is described. Then, the DPP operation using a bi-directional flyback converter operating in discontinuous conduction mode (DCM) is explained.

2.1 Architectures and Control Schemes

First, the optimal power processing method for isolated PV-to-bus architecture shown in Figure 1.8 and [18] is explained. Then, it is followed by other sub-optimal approaches and architectures.

2.1.1 Optimal Control

Figure 2.1 shows a single PV module with three subMICs forming the isolated PV-to-bus architecture. The subMICs are isolated bi-directional DC-DC converters. It is assumed that V_{str} is controlled to be at MPP by the central inverter.

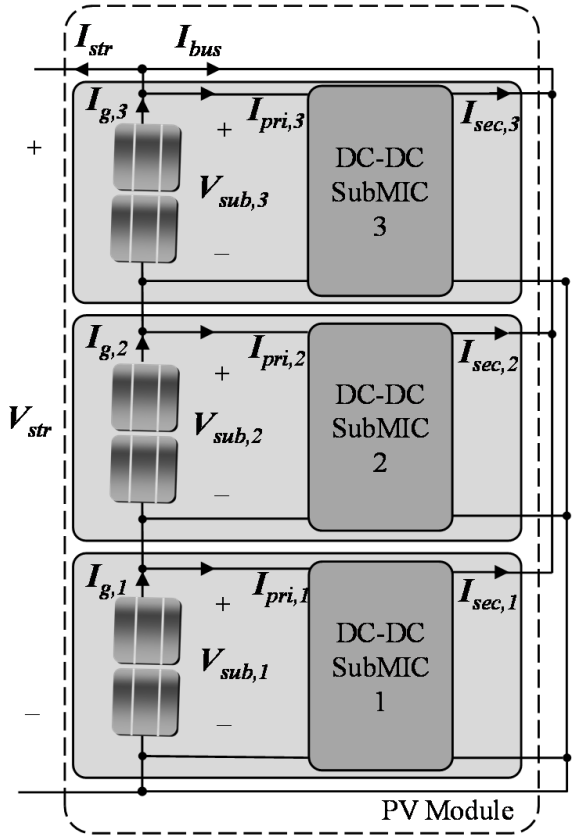


Figure 2.1: Isolated PV-to-bus architecture.

If the subMICs control $V_{sub,i}$ to operate the substring at MPP, $I_{g,i}$ can be determined. Then, the following linear equations can be solved to find the bus current (I_{bus}) and string current (I_{str}).

$$\begin{aligned} I_{pri,2} - I_{pri,1} &= I_{g,2} - I_{g,1} \\ I_{pri,3} - I_{pri,2} &= I_{g,3} - I_{g,2} \\ &\vdots \\ I_{pri,n} &= I_{str} + I_{bus} - I_{g,n} \end{aligned} \tag{2.1}$$

The set of equations in 2.1 does not have a single solution due to many possible I_{bus}. Optimally, a solution with minimal power processed through the subMIC would be desired. A

minimal power processed case can be found among the solutions:

$$P_{subMICs,min} = min\Big\{ \sum_{i=1}^{n} V_{sub,i} \mid I_{pri,i} \mid \Big\} \tag{2.2}$$

This is the optimal power processed by the isolated PV-to-bus architecture.

Although the optimal control method provides maximum performance, it has a disadvantage in the perspective of implementation. A centralized controller is required to communicate with all subMICs to ensure minimum processed power. PV system structure varies with each installment. The central controller would have to be flexible and adaptive to be fit for all PV system structures without increasing complexity.

2.1.2 Sub-optimal Control

A distributed control method not requiring central control is discussed in this section [1]. Potentially, the method enables a DPP system that is flexible to any module arrangements in a PV system. However, the power processed would not be optimal, hence it is called sub-optimal.

First, assume that all the substrings that are connected to the subMICs have matching characteristics. Then, it can further be assumed that the maximum power point voltage of the substrings (V_{MPP}) are close in value. Also assume V_{str} is fixed at the string level MPP voltage ($V_{MPP,PV}$). If all substrings are operating at MPP, let I_{str} be the average of the substring currents.

$$I_{str} = \frac{\sum_{i=1}^{n} I_{g,i}}{n} \tag{2.3}$$

Then, current through the primary side (I_{pri}) of the subMIC would equal to

$$I_{pri,i} = I_{str} - I_{g,i} \tag{2.4}$$

Now let a control with high finite gain ($K(s)$) force $v_{sub,i}$ to match V_{MPP}, determining $i_{pri,i}$.

$$i_{pri,i} = K(s)(V_{MPP} - v_{sub,i}) \tag{2.5}$$

The total power processed in the subMICs can be found from:

$$P_{subMICs} = V_{MPP} \sum_{i=1}^{n} \mid I_{str} - I_{g,i} \mid \tag{2.6}$$

Comparing the power processed in the subMICs between the optimal and sub-optimal control, the sub-optimal control at the worst case, can process two times more power. This is the case where mismatched substrings generate zero power [1]. In typical mismatch scenarios, the power processed would not be so different between the two control methods.

In the sub-optimal approach, I_{str} is the average of the substring currents. This is shown in equation 2.3. Then, all current processed in the isolated bus (I_{bus}) is zero. Hence, the isolated bus can be removed from the PV bus. The isolated-port PV-to-bus architecture in [1] uses this as an advantage for the sub-optimal control. Now the isolated bus voltage does not have to be at the high PV bus voltage. The isolated-port PV-to-bus architecture is shown in Figure 2.2.

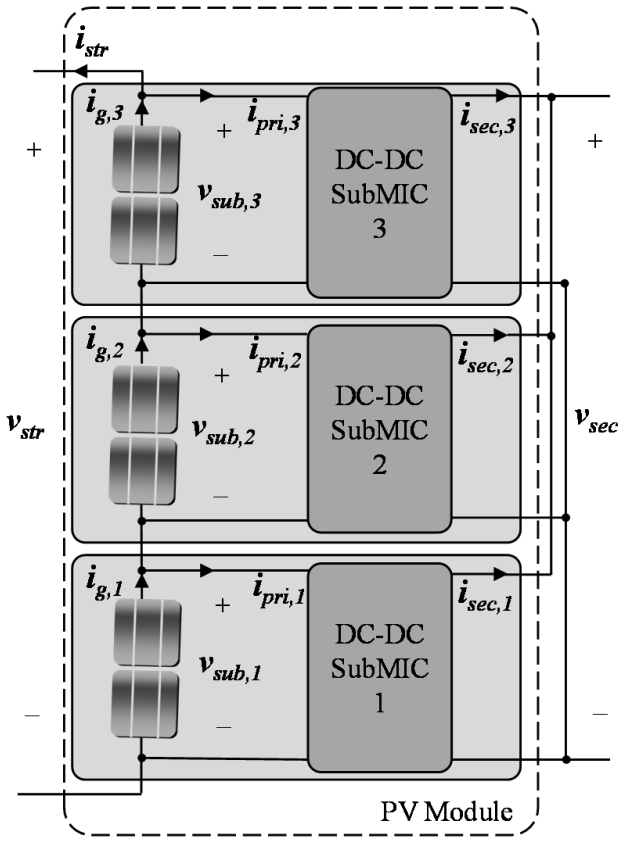


Figure 2.2: Isolated port PV-to-bus architecture with the auxiliary bus isolated with its voltage independent of the PV bus.

2.1.3 Voltage Balancing Control

In Section 2.1.2, the sub-optimal control method was explained. Also, it shows that the auxiliary bus for power balancing does not need to be connected to the high voltage PV bus.

Although the net power in and out from the isolated bus would be zero, the voltage of the bus (V_{sec}) is not determined. If we assume the voltage is also equal to V_{MPP}, then $I_{pri} = I_{sec}$ would be also true. Furthermore, by observing where V_{MPP} is in the IV curve of a PV substring, the current to voltage slope around the actual V_{MPP} does not vary much with power variations. This is shown in Figure 2.3. Also, the power variations versus voltage is

small near the V_{MPP} point. Given that the subMICs will operate with $V_{sub,i} \approx V_{MPP}$, the

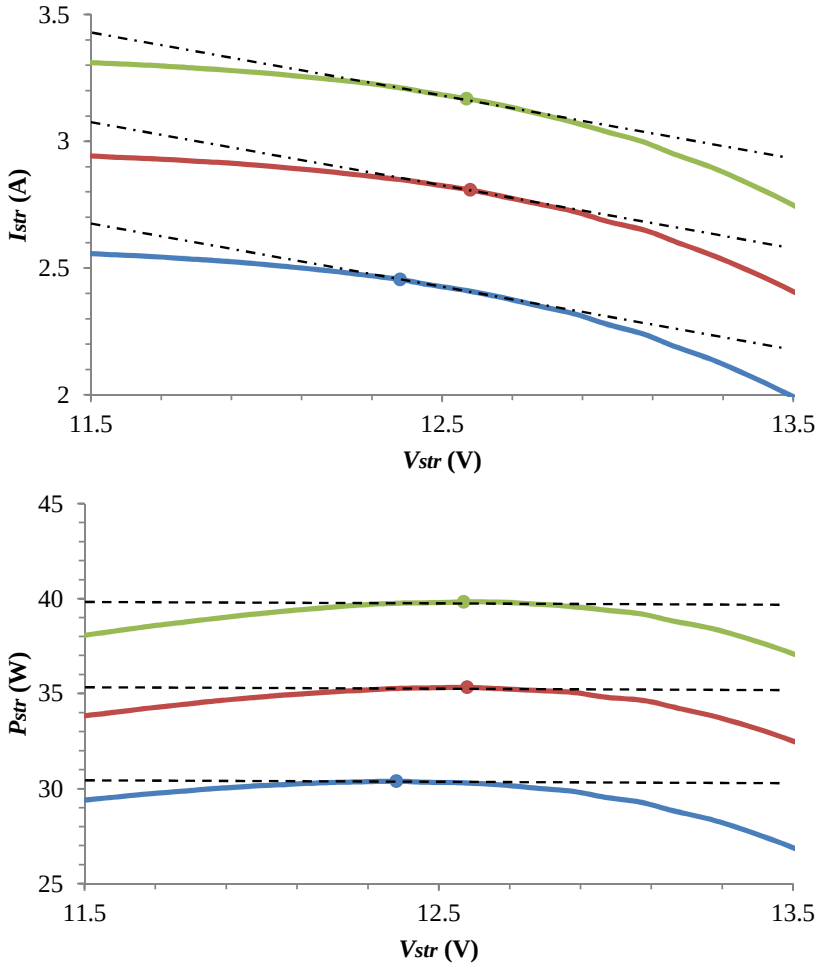


Figure 2.3: IV (top) and PV (bottom) curve of PV substrings with 25% power variations showing identical tangent lines (dot-dash, dot) overlaid over the V_{MPP} point.

string current and string voltage can be seen to be linear and inversely proportional. Then, assuming the subMICs have a 1:1 voltage conversion ratio for the isolation transformer, we can define the following control law which is dependent on the difference of subMIC port voltages, where $K(s)$ is of finite gain.

$$i_{pri,i} = K(s)(v_{pri,i} - v_{sec}) \tag{2.7}$$

2.2 Voltage Balancing with Bi-directional Flybacks in DCM

The flyback converter is a buck-boost type converter with isolation due to the flyback transformer present in the topology. It is easily modified to be a bi-directional converter as shown in Figure 2.4.

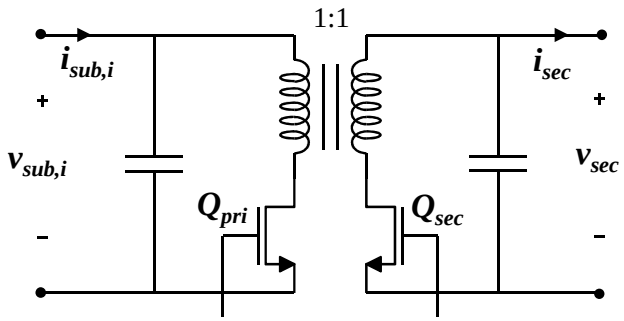


Figure 2.4: Bi-directional flyback topology used for the subMIC power stage with MOSFET switches.

The topology uses only two semiconductor switches and a single magnetic component, which makes it attractive as a cost effective solution. The drawbacks of the topology is that the semiconductor is exposed to high voltages during switching off transition. Also, the flyback transformer is designed as an energy storage device which only delivers energy at one of the switching phase.

If the flyback is operated in discontinuous conduction mode (DCM), the input can be seen as a lossless resistor and the output of the converter can be seen as a power source [22] in a large signal averaged model. With reference to the topology shown in Figure 2.4, when Q_{pri} MOSFET is on, the current on the primary inductance (L_{pri}) is ramped up. When the MOSFET is turned off, the current ramps down while the body diode of Q_{sec} MOSFET conducts the current until it reaches zero. Duty cycle d_{pri} is defined as the duty ratio that the MOSFET is on for a given switching period (T_s). Then, the lossless resistance (R_e) and

the input current (i_{pri}) are of the following:

$$R_e = \frac{2L_{pri}}{d_{pri}^2 T_s} \tag{2.8}$$

$$i_{pri} = \frac{v_{sub}}{2L_{pri}} d_{pri}^2 T_s \tag{2.9}$$

Extending the analysis to a bi-directional perspective, the duty cycle to current relationship can be obtained.

$$\begin{aligned} i_{pri} &= v_{sub} \frac{T_s}{2L_{pri}} d_{pri}^2 \\ i_{sec} &= -v_{sec} \frac{T_s}{2L_{pri}} d_{sec}^2 \end{aligned} \tag{2.10}$$

Current is proportional to the square of the duty cycle. If the duty cycles were to be controlled with the port voltage difference as in equation 2.7, the port currents would be proportional to the square of the port voltage difference. Given the assumption of linearized and constant current to voltage relationship from Section 2.1.3, the following control scheme for the bi-directional flyback can be expected to achieve sub-optimal DPP performance when v_{sub} and v_{sec} are very close.

$$\begin{aligned} d_{pri} &= K_p(s)(v_{sub} - v_{sec}) \ , \ when \ v_{sub} > v_{sec} \\ d_{sec} &= K_p(s)(v_{sec} - v_{sub}) \ , \ when \ v_{sub} < v_{sec} \end{aligned} \tag{2.11}$$

Gain $K_p(s)$ is important in this control scheme. However, it does not impact system performance significantly as long as $K_p(s)$ is sufficiently high [23].

Chapter 3

Design Realization of SubMICs

In this chapter, realizing the design of the bi-directional flyback subMICs is discussed. In a DPP system , the efficiency of the converter has less impact on the PV system efficiency than the full power processing methods. However, efficiency is still important and the converters must be designed with weight on low power efficiencies. At the same time, the converter size and cost must be minimized for PV applications.

First, the flyback power stage is discussed. Then the design and loss evaluation of planar transformer is presented. Next, the custom controller IC design and features implemented to improve efficiency are discussed. Finally, the prototype board is presented.

3.1 Power Stage

The power stage selected for the subMIC is a bi-directional flyback operating in DCM. Some of the critical design specifications are shown in Table 3.1.

Maximum port voltages	:	16 V
Maximum port current	:	3 A
Minimum control bandwidth	:	1 kHz

Table 3.1: Design specifications

Other than the electrical specifications, the converter would be required to fit in a PV

module junction box. It must be sufficiently small and thin. It should also be capable of operating at high load with sufficient efficiency while maintaining the efficiency at very low load. Low load efficiency is particularly important because the processed power distribution will be similar to a laplacian distribution weighted towards low power. Another important consideration to take into account is insertion loss. The converter and its controls should not contribute to power loss when no power processing is required. Hence, minimizing the quiescent power consumption of peripheral circuits is important. The selected flyback power stage is shown in Figure 3.1.

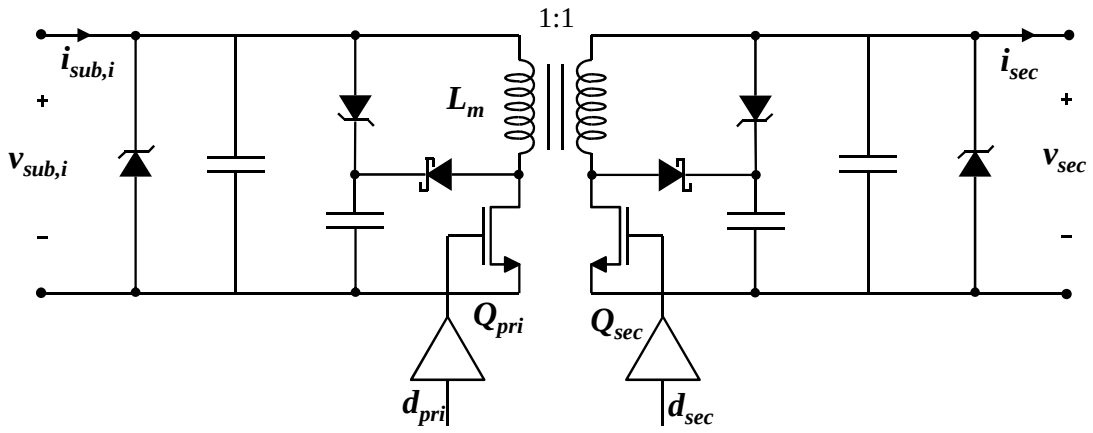


Figure 3.1: Bi-directional flyback topology with snubbers for a subMIC.

The converter transformer winding ratio is 1:1, keeping v_{sub} and v_{sec} at the same voltage scale. Ports are protected with zener diodes to ensure the port voltages do not exceed 18 V. The MOSFETs are exposed to at least two times the maximum port voltage, 32 V. The voltage can rise higher due to voltage spikes during turn off. Zener type snubbers are used to ensure that the MOSFETs are not exposed to excessive voltages while minimizing light load efficiency drops. The Zener voltage is set to be lower than the MOSFET rating, and higher than 32 V. MOSFETs are rated to be at 80 V. The PWM switching frequency is 100 kHz.

3.2 Loss Modeling

Loss estimation method for the subMIC design is presented. The losses are categorized by the dependency on switching frequency and the inductor. Typically, the DCM flyback losses can be divided into the following losses shown in Table 3.2.

Conduction losses :	P_{Ron} :	MOSFET conduction loss when switch is on
	P_{diode} :	MOSFET conduction loss when body diode conducts
Switching losses :	P_{gate} :	Gate charge loss
	P_{coss} :	Switching loss due to switch node capacitance
	P_{leak} :	Switching loss due to leakage inductance
Magnetic losses :	P_{Ldc} :	Inductor DC copper loss
	P_{Lac} :	Inductor AC copper loss
	P_{core} :	Core loss

Table 3.2: Loss type classification for the DCM flyback

Since the converter is symmetric, loss modeling is explained with power flowing from the primary side to the secondary side of the converter.

3.2.1 Conduction Loss

The DCM flyback operates with zero current at the beginning of a switching period (T_s). When the primary side Q_{pri} is turned on, the current through the MOSFET is ramped up until the switch is turned off, forming a triangular waveform with a peak current (I_{pk}). The duration of this phase is $D_1 T_s$. Then, the current is conducted on the other side of the winding through the body diode of Q_{sec}. The current ramps down from I_{PK} to zero in $D_2 T_s$. The conduction losses can be defined as the following:

$$P_{cond} = I_{pk}^2 \frac{D_1}{3} \cdot R_{on} \tag{3.1}$$

$$P_{diode} = I_{pk} \sqrt{\frac{D_2}{3}} \cdot V_{sec} \tag{3.2}$$

where,

$$I_{pk} = \frac{V_{pri}}{L} D_1 T_s \tag{3.3}$$

$$D_2 = I_{pk} \frac{L}{V_{sec} T_s} \tag{3.4}$$

3.2.2 Switching Loss

Gate charge related loss is from the gate charge required to turn on the MOSFET. This energy is lost when the MOSFET is turned off. Given the gate charge of the MOSFET (Q_g) at a given driving voltage V_{gate}. The gate drivers loss can be estimated by Equation 3.5. The power loss associated from the gate driver power supply and the circuits associated with the drivers are neglects.

$$P_{gate} = Q_g \cdot V_{gate} \cdot f_s \tag{3.5}$$

Switch node capacitance loss is also related to the MOSFET device and parasitic capacitances. If the capacitances seen at the drain of the MOSFET are lumped together as C_{oss}, the loss can be estimated as in Equation 3.6.

$$P_{coss} = \frac{1}{2} C_{oss} (V_{pri} + V_{sec})^2 \cdot f_s \tag{3.6}$$

Assume the MOSFET turn off speed is much faster than the ramp of the leakage inductance (L_{lk}) current to zero. Then, it can be assumed that the leakage current (i_{lk}) is all dissipated through the zener clamping diode in the snubber. The power loss can be calculated as Equation 3.7.

$$P_{leak} = \frac{1}{2} I_{pk} V_{zener} \cdot T_x \cdot f_s \tag{3.7}$$

where T_x is the time that it takes for i_{lk} to ramp down from I_{pk} to zero.

$$T_x = I_{pk} \frac{L_{lk}}{V_{zener} - V_{sec}} \tag{3.8}$$

3.2.3 Magnetics Loss

The flyback transformer consists of multiple windings which transfers power over one winding to another. It acts more like an inductor. The stored energy is transfered between the windings. In a DCM flyback, only one winding conducts current at a given time. When Q_{pri} is on, the current flows through the primary side winding. When it is turned off, current flows through the secondary side winding, until the current reaches zero.

If $R_{Ldc,pri}$ is the primary side winding resistance and $R_{Ldc,sec}$ is the secondary side winding resistance, the DC copper loss of the magnetic component can be estimated similarly as the MOSFET conduction loss since the winding currents are equal to the MOSFET currents.

$$P_{Ldc,pri} = I_{pk}^2 \frac{D_1}{3} \cdot R_{Ldc,pri} \tag{3.9}$$

$$P_{Ldc,sec} = I_{pk}^2 \frac{D_2}{3} \cdot R_{Ldc,sec} \tag{3.10}$$

where I_{pk} and D_2 are found in Equation 3.3 and 3.4.

The AC portion of the current generates fields around the copper, contributing to other conduction losses. These losses can be classified into eddy current loss, winding proximity loss, and airgap fringing flux related losses. Much work are done in estimating these losses, but the loss calculation is relatively complex and must consider the underlying assumptions made in the calculations [22, 24–26]. Proximity loss considering frequency decomposition for the flyback transformers have been investigate in [27, 28]. Studies in [29, 30] show how AC copper loss due to airgap fringing can be estimated and also suggests what is required to minimize the losses.

Instead of using the methods used in the literatures, 2-D finite element method simulation, FEMM [31], is used to estimate the AC related copper losses. A cross-section of the flyback transformer is analyzed through frequency decomposition. Then the equivalent AC resistance for each decomposed frequency component is found. Next, the AC copper

resistance is extrapolated to the mean length turn (MLT) of the winding. Finally, loss is summed up as the following.

$$P_{Lac,pri} = \sum_{n=1}^{harm} I_{pk,n\cdot f}^2 R_{Lac,pri,n\cdot f} \tag{3.11}$$

$$P_{Lac,sec} = \sum_{n=1}^{harm} I_{pk,n\cdot f}^2 R_{Lac,pri,n\cdot f} \tag{3.12}$$

The core loss can be estimated using the piecewise waveform analysis using Steinmetz parameters [32]: the improved Generalized Steinmetz Equation (iGSE). This method uses the usual Steinmetz parameters for a material:

- K_{fe} : core loss coefficient
- α : frequency exponent
- β : density flux exponent

The Steinmetz model is known to be a good choice for modeling core loss. However, it assumes the signal is a sinusoidal waveform. The iGSE method includes the high frequency component of the waveform for improved accuracy. Core loss is calculated as Equation 3.13.

$$P_{core} = \frac{1}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^a (\Delta B)^{\beta-\alpha} dt \tag{3.13}$$

where

$$k_i = \frac{K_{fe}}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^\alpha \, 2^{\beta-\alpha} d\theta} \tag{3.14}$$

However, this method does not consider affects from DC bias.

3.3 Planar Magnetics

The magnetic component is the largest component in the subMIC. It determines the overall height of the subMIC. Planar magnetic design on PCB allows the windings to be of lower height. Also the windings can be reproduced to be close to identical. Another

advantage is that the core can be place right on the PCB. However, the planar multilayer winding has some disadvantages. First, the planar windings stacked up in planes form nice capacitive plates. The capacitance can degrade inductive performance and also allow high frequency current across the transformer isolation.

Few selected set of designs are produced to compare the actual performance of the magnetics to the loss models. Designs are selected based on the optimal design selection based on the loss estimates. Core selection and winding configurations are varied in the set. Target inductance for the power stage is 7-8 μH, switching frequency is 100 kHz, and the peak current in the magnetic is expected to be safe at 10 A.

In this section, candidate magnetic designs are selected for loss estimation. Then, optimal designs are manufactured as final candidates for the subMICs.

3.3.1 Core Selections

Through rough analysis, a family of ferrite cores from TDK are selected. The selected material for the core is the PC95 material, which has stable loss characteristics versus temperature. The core loss is expected to be relatively low for this material. Saturation flux density is 410 mT at 100 C, and the loss density is estimated to be 300 kW/m^3 at 200 mT and 100 kHz. Flat ELT type cores that are specific to PCB planar design are selected. For comparison of size, a POT type core is shown with ELT core candidates in Figure 3.2. The specifications of the selected ELT cores are shown in Table 3.3.

Given the maximum operating point and specifications for the power stage, the peak flux densities are evaluated in Table 3.4. The results show that minimum of 4 turns will keep the core out of saturation range for 20 and 22 size cores. For further evaluation, cores size 20 and 22 are considered. Also, turns of 4 or more are considered.

The cores will have an airgap at the junction of the E and I shaped core. The core comes in two winding heights: 2 mm and 4 mm.

Multiple layer PCBs will be used for the windings. If the overall height of the planar

ELT20x7 ELT22x8 POT2213

Figure 3.2: TDK ELT type cores for the design and a POT core.

	A_e(mm^2)	l_e(mm)	A_L(nH/N^2)
PC95ELT18X7.3-Z	44.3	23.8	4760
PC95ELT20X5.7-Z	54.9	21.6	6270
PC95ELT20X7.7-Z	54.6	25.6	5630
PC95ELT22X6-Z	66.6	23.4	7250
PC95ELT22X8-Z	66.2	27.3	6540

Table 3.3: Specifications for TDK ELT type cores. Effective core area A_e, length l_e, and the inductance per wind estimation factor A_L is shown.

Bmax(mT)	Turns					
	3	4	5	6	7	8
PC95ELT18X7.3-Z	602	452	361	301	258	226
PC95ELT20X5.7-Z	486	364	291	243	208	182
PC95ELT20X7.7-Z	488	366	293	244	209	183
PC95ELT22X6-Z	400	300	240	200	172	150
PC95ELT22X8-Z	403	302	242	201	173	151

Assume fs=100kHz, Ipk=10A, L=8uH

Table 3.4: Worst case flux density for the cores are given for several candidate turns. Green denotes flux density is below 70% of saturation and red denotes that the core would saturate.

winding is too thin, parasitic capacitance increases. If the height increases, the windings become closer to the airgap.

According to [26], the loss due to airgap fringing flux is dependent on the airgap length and distance between the airgap, versus the copper distance from the airgap. It is found in later sections that the copper windings should be more than 2 mm away from the airgap to minimize airgap related loss. Considering the thickness of high ounce copper and insulation material between the copper, it is difficult to use the 2 mm height window for multiple layer PCB with high ounce copper. The 4 mm height window provides more flexibility in design with the trade off of larger core volume. The 4 mm height cores are considered for the designs. This corresponds to the ELT20x7.7 and ELT22x8 cores.

3.3.2 Winding Selections

Winding of the magnetics are designed on the copper layers of a PCB. The design can have multiple turns of winding on a single PCB layer or have multiple PCB layers for multiple turns. Due to the small geometry of the core, single turn per PCB layer is used for the prototype design. Even a two turn per layer winding would be hard to design due to the vias required near the center of the winding. It would only be possible to fit one or two minimal sized vias. The winding structure relative to the core are shown in Figure3.3.

From the winding configuration chosen, whether to interleave the winding layers or not can be decided. In transformers, wire interleaving is used to minimize proximity losses. The opposing current direction of each transformer winding mitigates the MMF build between the windings. The trade-off of this is the increase of parasitic inter-winding capacitance. In the DCM flyback, only one of the windings conduct current at a given time. The benefit of interleaving would be weak. Performance analysis of interleaving is done in FEMM using the 2-D cross-section of the magnetics. The analysis compares the AC copper loss of a 5 turns per winding case. Loss is evaluated for a 4 A peak sinusoidal at 100 kHz. The stack is designed with the secondary side winding on the bottom most side closest to the core, then stacked up. Both primary and secondary side excitation is compared. Loss evaluated is the sum of both winding losses for a given scenario. FEMM results are shown in Figure 3.4.

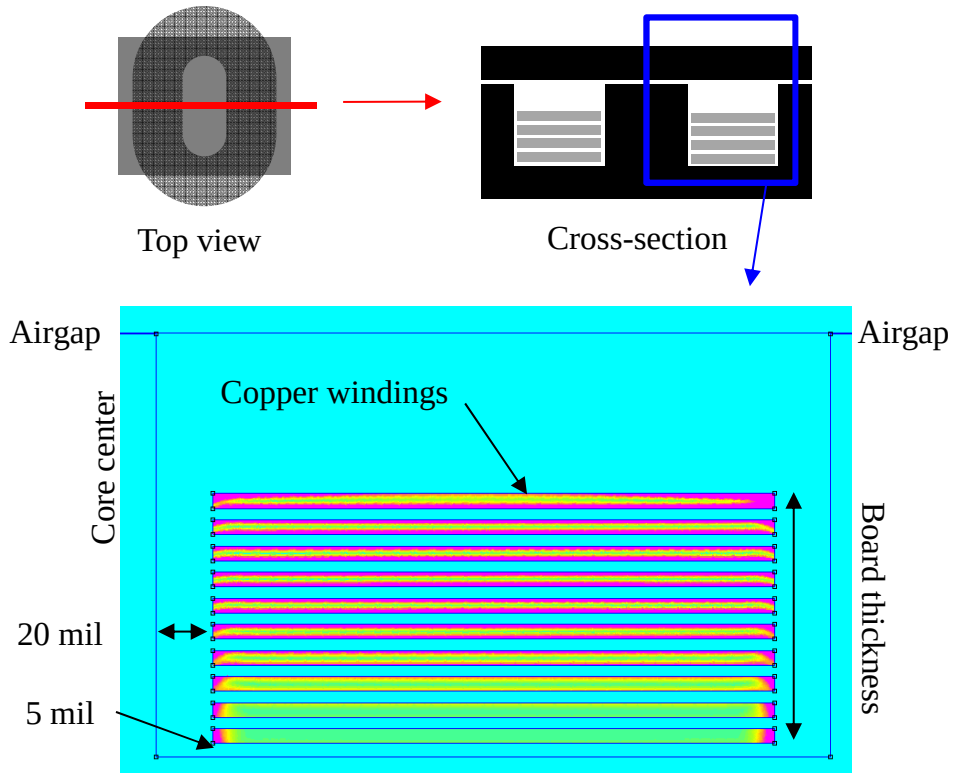


Figure 3.3: Diagram of core and winding structure with key design geometries shown.

Results show that interleaving does not improve AC related loss significantly. It also shows that it could worsen the loss very slightly in the secondary side conduction phase. The benefit from interleaving the windings is small while the complexity of designing the PCB would increase. The analysis suggests that the copper winding location is more relevant to loss than whether or not interleaving is used. Therefore, interleaved winding is not considered in the design.

Next, the board thickness is determined. For the design, only turns of 4 or more are considered for the winding designs. Given that 5 turns per winding is chosen with 4 oz copper, the minimum board thickness possible would be of 93 mil. FEMM analysis is performed for 93 mil and 125 mil board thicknesses to analyze loss increase related to the airgap. The 125 mil case has the minimum distance from the airgap reduce by half compared to the 93 mil

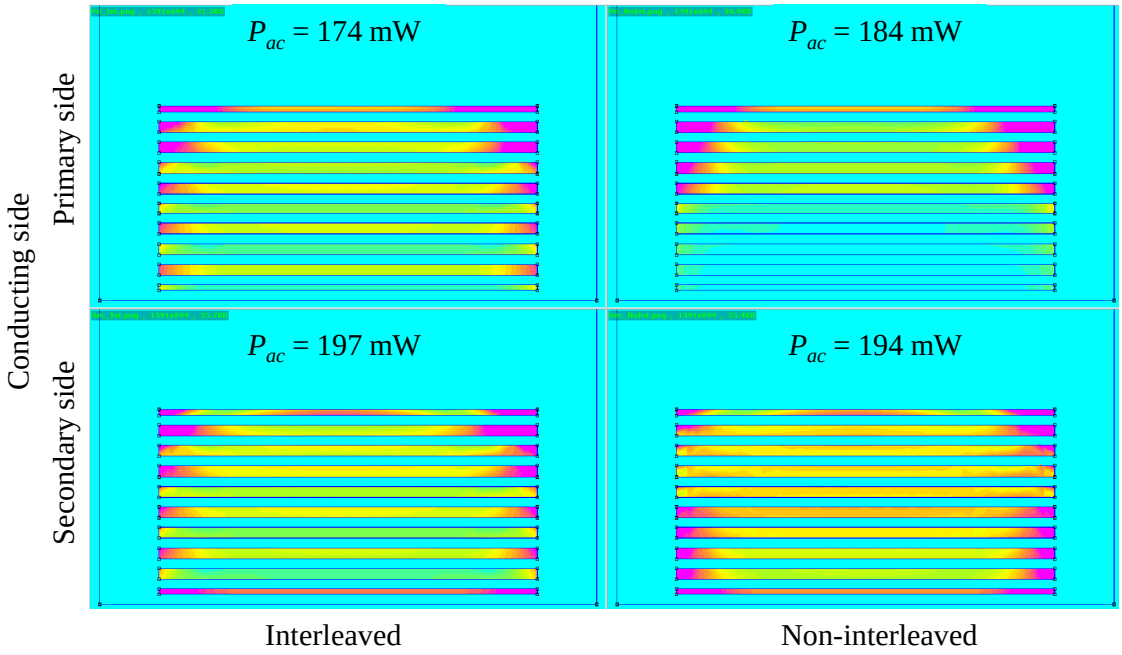


Figure 3.4: FEMM analysis results comparing interleaved (left column) and non-interleaved (right column) AC copper loss when excited with a 4 A, 100 kHz sinusoidal current in the primary side winding (top row) and secondary side (bottom row). Magenta indicates higher current densities and cyan indicates the lowest current densities.

board. For the analysis, the secondary side winding on the bottom side is excited with a 4 A peak sinusoidal at 100 kHz. Figure 3.5 shows the results. Loss is evaluated in the same manner as the analysis done for the interleaved winding case.

Results show that the AC copper loss doubles for the 125 mil board. Considering that there is proximity and eddy current losses already present in the total loss, loss contribution from the airgap fringing flux is very significant. Visually analyzing the results, increase in current density due to the airgap is already observed in the top corners of the 93 mil thick board. Therefore, only copper ounces below 4 oz and 5 turns are considered for the design.

3.3.3 Loss Estimations

Loss evaluation are performed for selected design sets considered in the previous section. Loss estimates are evaluated for the combination of following design variations:

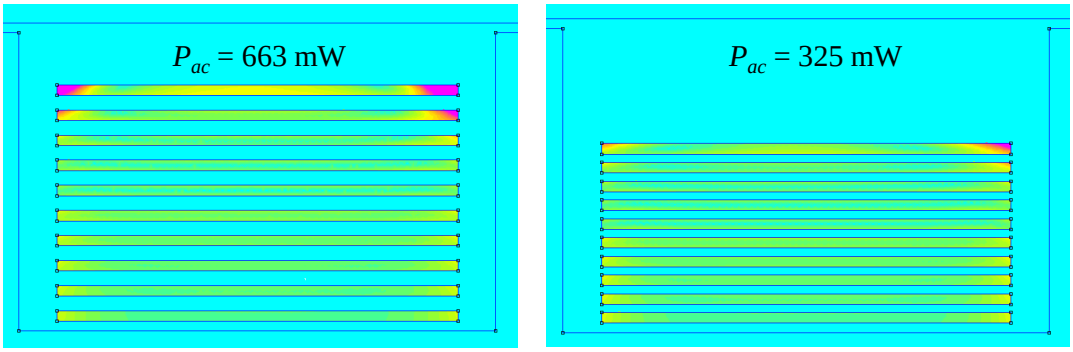


Figure 3.5: FEMM analysis results comparing AC loss dependent on the distance from the airgaps while the bottom winding is excited with current.

- Cores : ELT20x7 and ELT22x8 cores with PC95 material
- Copper ounce : 2, 3, and 4 oz copper
- Winding turns : 4 and 5 turns per winding
- Board thickness : 93 mil

Loss Estimation Method The losses are evaluated the methods presented in Section 3.2.

Core loss is evaluated using the *i*GSE method. Loss calculation is performed using the corresponding peak flux density B. Core loss parameters are extracted for temperature of 60 C.

DC resistance is evaluated by using the MLT of the copper winding as the length of the winding, and winding plate cross-section as the cross-section area of the winding. Copper resistivity at 100 C is used.

DC loss is calculated by doubling the loss from a single winding. This is possible due to the symmetric design of the two windings. Identical current waveform on the two current

phase is assumed.

AC loss is analyzed by obtaining AC resistance from FEMM simulation of the core cross-section. Then, the resistance is extrapolated to the MLT of the winding. The AC current component is decomposed into harmonic magnitudes for loss calculation. Each AC loss consists of sum of losses from 20 harmonics. Depending on the duty cycle of the current waveform, error could be up to 25% when compared to loss considering 200 harmonics [27]. Losses from the two winding phases are summed for the total AC loss.

ELT20x7 Core, Loss Estimation Results

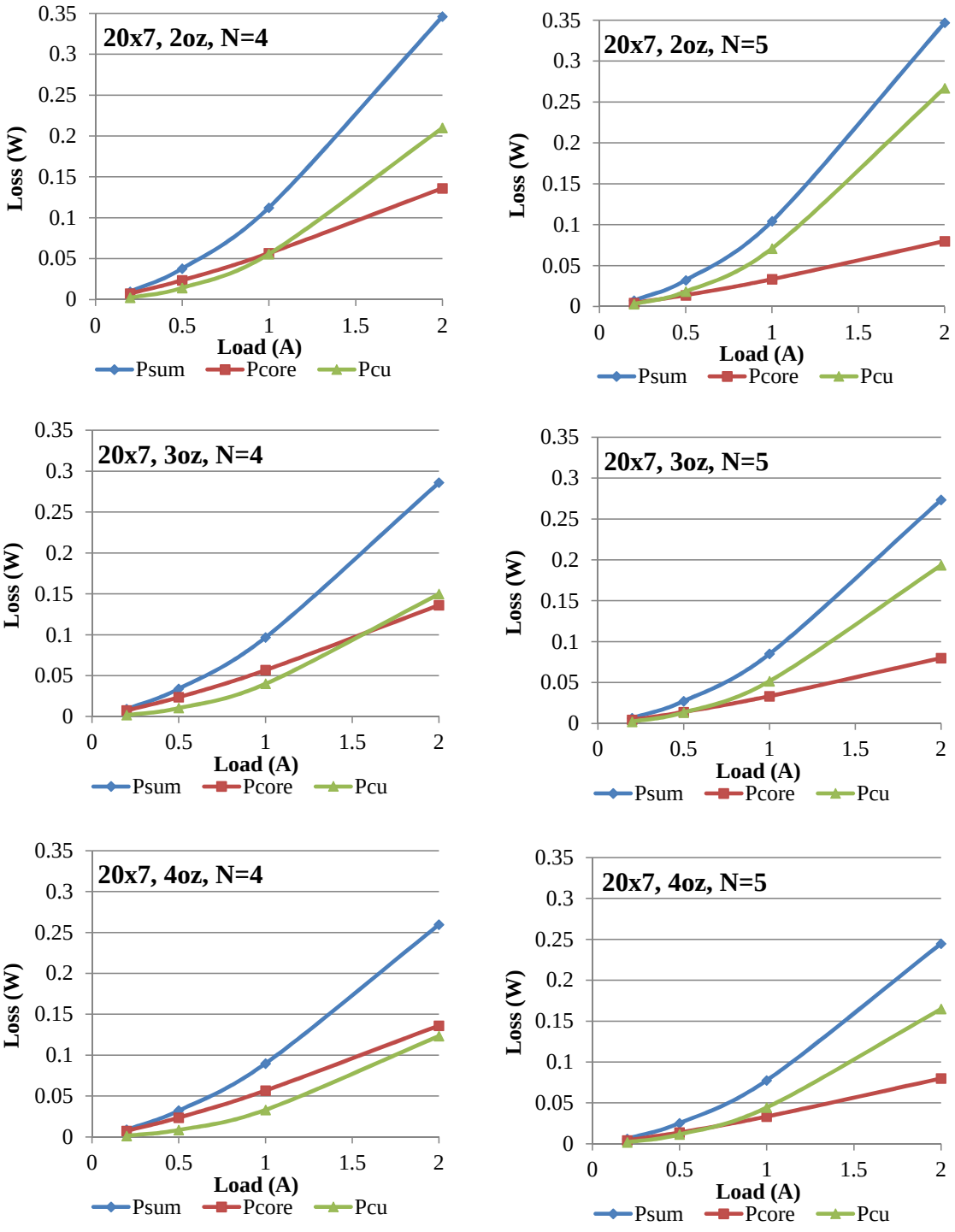


Figure 3.6: Loss estimation for the planar magnetic designs using ELT20x7.

ELT22x8 Core, Loss Estimation Results

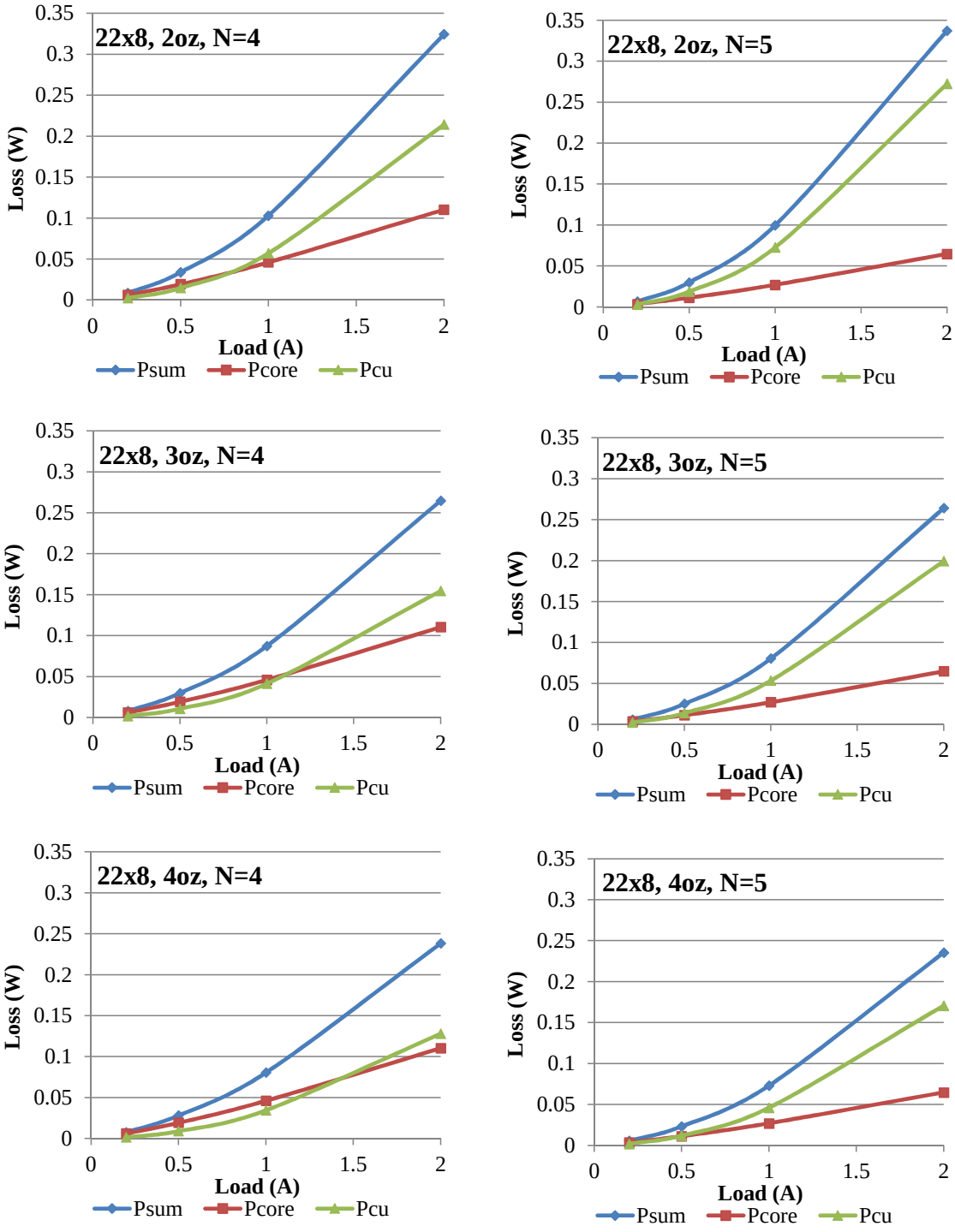


Figure 3.7: Loss estimation for the planar magnetic designs using ELT22x8.

Result Analysis Results show that 5 turns per winding is optimal for all configurations. Also, thicker copper is better given that the board thickness can stay the same and the parasitic capacitance is not considered. The two cores show little difference in total loss. However, loss distribution could be different in the manufactured design. Therefore, we could consider both cores for the subMIC design. 3 and 4 oz copper show similar performance, so both could also be considered. The 3 oz board could be manufactured with a thinner board.

The planar winding PCBs are manufactured for both 20 and 22 size cores. It is a 10 layer board with 110 mil thickness on a single PCB. The planar winding designs can be separated from the combined PCB, then attached to the subMIC PCB for evaluation. Since all design will be on one board, copper thickness would have to be the same.

However, a manufacturing problem arose. Even with 3 oz copper, the thinnest possible thickness of the board that can be manufactured was at minimum of 100 mil. Loss contribution of the airgap is significant if the board is to be thicker. Hence 3 oz copper is selected. The choice does not affect optimization significantly since the loss estimates showed that there is not much performance difference to the 4 oz designs.

3.3.4 Realization

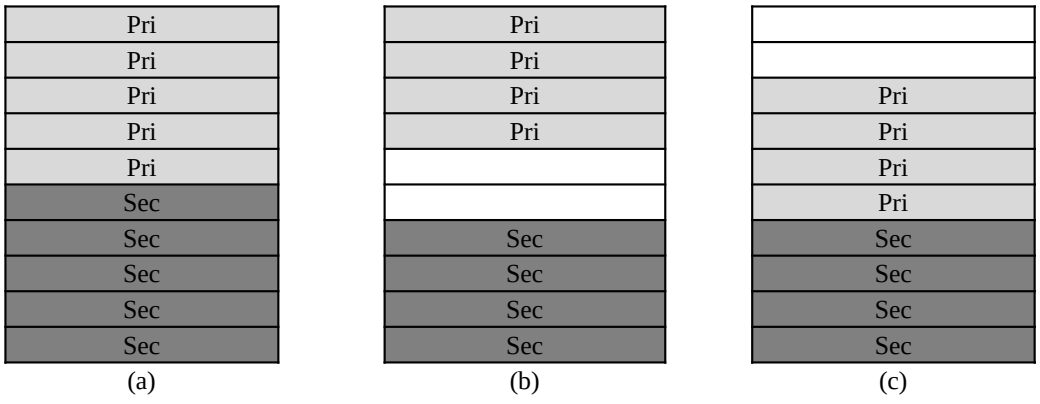


Figure 3.8: Planar windings stack configurations.

Figure 3.8 shows how the PCB copper layers are configured. Configuration (a) is the 5 turns per winding version. Configuration (c) is the 4 turns per winding version, which emulates a thinner PCB thickness by not using the top most two PCB layers. Configuration (b) will be used to compare performance with (b). The winding configurations will be defined as the following throughout the following chapters:

- Design (a) : 20-55 and 22-55
- Design (b) : 20-424 and 22-424
- Design (c) : 20-442 and 22-442

The planar winding PCB layout is shown in Figure 3.9. The routing between the winding layers are done through multiple vias on the outer edges. End terminations are made so that it could be easily placed and removed from the subMIC board.

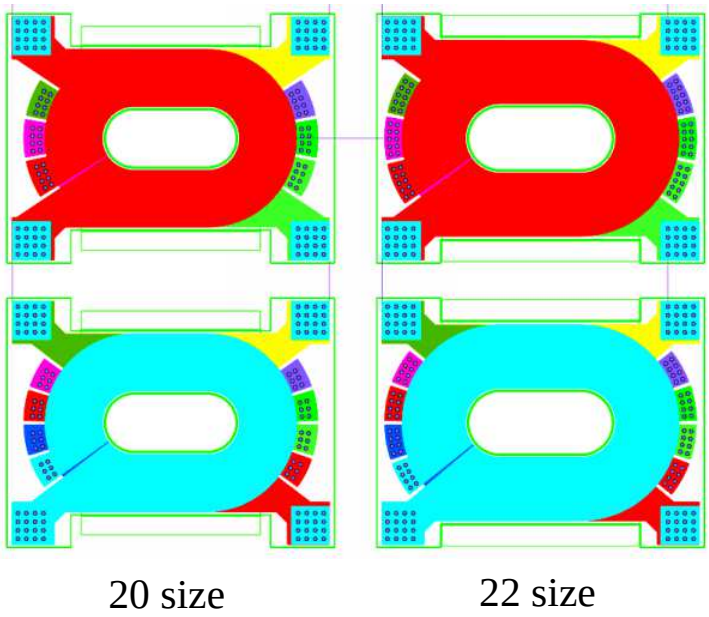


Figure 3.9: Planar PCB layout.

The final designs manufactured are shown in Figure 3.10.

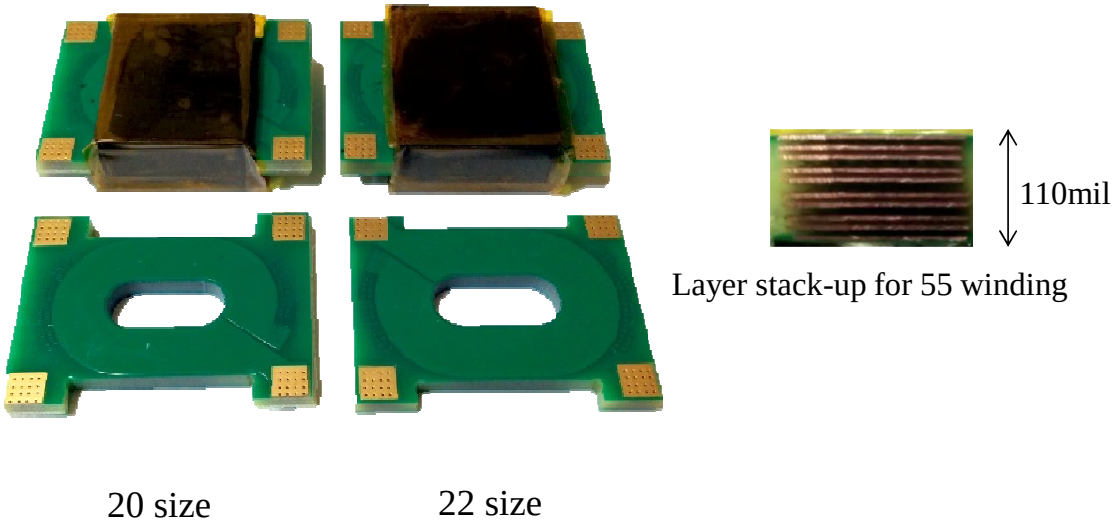


Figure 3.10: Planar magnetics designed for the subMICs.

3.4 SubMIC Controller IC

A single controller IC can be used to integrate many of the functions required for the subMIC. The prototype subMIC controller IC includes the key functions for voltage balancing control, power limiting, and modes for loss optimized controls. It also includes a voltage to PWM conversion feature for dual use as secondary side voltage sensing IC. SubMIC board with the IC controller is shown in Figure 3.11.

3.4.1 Modes of Control

The subMIC operates with four modes of control [3]. The main operation would be performing the linear control described in Section 2.2. Also, the controls can limit the power processed by limiting the gain of the converter or by completely shutting it down, allowing the converter to operate safely at low power rated designs. Also, the converter is turned off when there is not much need for power balancing. The modes of operation used are defined as the following four:

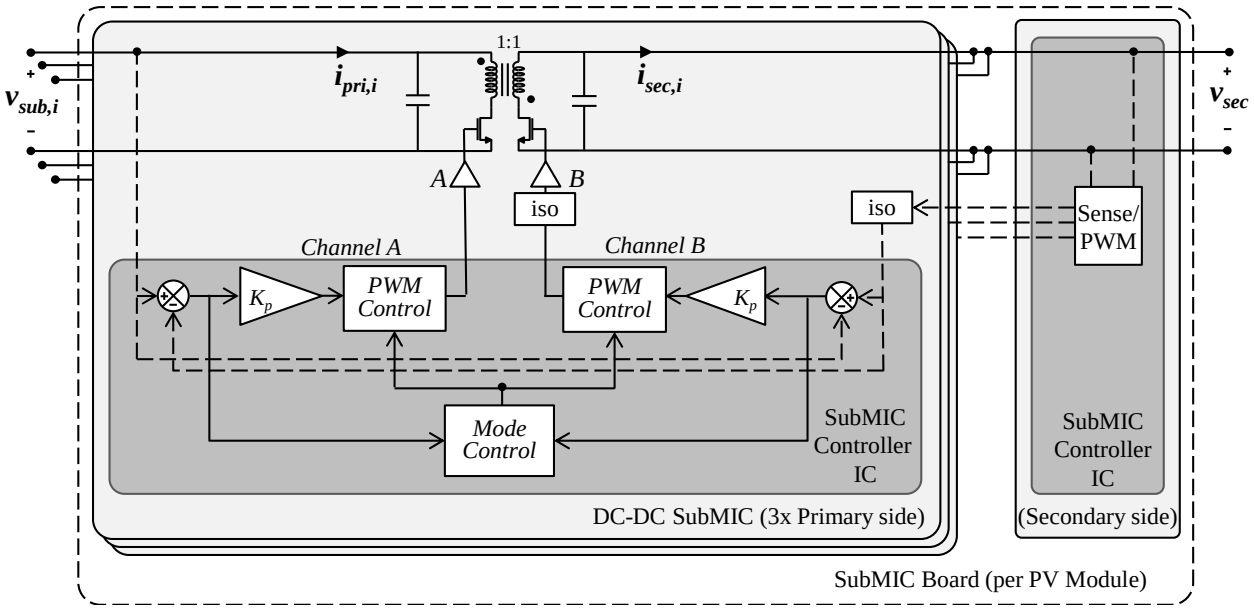


Figure 3.11: Structure of the subMIC prototype with the controller IC.

- Off : The converters are turned off.
- $Linear$: Operates with the voltage balancing scheme.
- Sat : The converter operates with limited gain, limiting power processed.
- $Limit$: The converters are turned off, limiting operation at high power.

Modes are determined on port voltage differences. Figure 3.12 shows a better insight of how the control modes relate to port voltage difference and duty cycles of the converter. Although the figure shows the sensed input to duty cycle output relationships, other features are also dependent on the control modes. In the following subsections, the control modes are explained in detail.

The Off Operation Having no insertion loss, the DPP subMIC system has an advantage over full power processing systems at low mismatch. Hence, it would be expected that the system efficiency would be near ideal when there is very little mismatch present.

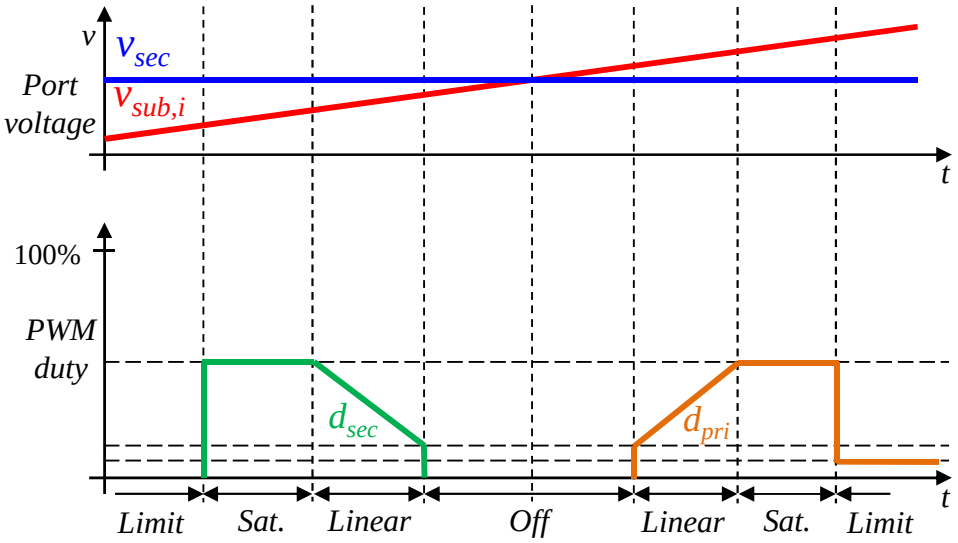


Figure 3.12: Output duty cycles with input voltage difference evolving over time .

This would not be true if the subMICs process the low power mismatches with low efficiency. For fixed frequency PWM operation, the DCM flyback efficiency is relatively low at low load.

The Off mode turns the converter off to prevent low power operation when port voltage difference is very low. Since the power processed in a DPP PV system is heavily weighted at low power, it may seem as that presence of the Off mode will degrade the overall system performance. However, this is not true do to the minimum duty cycle present in the next *linear* mode. The interacting subMIC controls in the system causes the subMIC to act like it is in a burst on-off control mode. The burst characteristics allow the converter to operate at a higher efficiency since the duty cycle of the pulses are at least at minimum duty cycle (D_{Lsat}) and the total switching cycles are lower than the PWM case.

The quiescent power consumption of the control circuits can also contribute to the insertion loss. In the Off mode, there is not much the controller IC is required to do. Loss can be minimized by shutting down unused blocks in the IC. However, shutting down or turning on the supplies contribute to mode transition delays. As a result, it contributes to

mode transition instability such as the burst characteristic. The operation can be expressed as following:

$$\begin{aligned} d_{pri,i} &= 0\ ,\ when\ v_{sub} - v_{sec} < V_{off} \qquad (3.15) \\ d_{sec,i} &= 0\ ,\ when\ v_{sub} - v_{sec} < -V_{off} \end{aligned}$$

$$(3.16)$$

The *Linear* Operation The *Linear* operation is the main mode of operation. The voltage balancing controls described in Section 2.1.3 is performed. This mode operates with high gain by controlling the duty cycle in scale to the port voltage difference. Combined with the Equation 3.15, equation for the two modes can be expressed as:

$$\begin{aligned} d_{pri,i} &= K_p(s)(v_{sub} - v_{sec})\ ,\ when\ v_{sub} - v_{sec} > V_{off} \qquad (3.17) \\ d_{sec,i} &= K_p(s)(v_{sec} - v_{sub})\ ,\ when\ v_{sub} - v_{sec} > -V_{off} \\ else\ ,\ d_{pri,i} &= d_{sec,i} = 0 \end{aligned}$$

The *Linear* mode includes the compensating function $K_p(s)$. The design of $K_p(s)$ determines the performances of the system: efficiency and stability [2].

The *Sat* Operation The *Sat* mode, or saturation mode, prevents the duty cycle determined from the *Linear* mode exceeding the maximum allowed duty cycle (D_{sat}), hence saturating the duty cycle. The combined equation is shown in Equation 3.18.

$$\begin{aligned} d_{pri,i} &= min(K_p(s)(v_{sub} - v_{sec}), D_{Hsat})\ ,\ when\ v_{sub} - v_{sec} > V_{off} \qquad (3.18) \\ d_{sec,i} &= min(K_p(s)(v_{sec} - v_{sub}), D_{Hsat})\ ,\ when\ v_{sub} - v_{sec} > -V_{off} \\ else\ ,\ d_{pri,i} &= d_{sec,i} = 0 \end{aligned}$$

The subMIC flybacks are designed to be operated in DCM mode. The duty cycle limit helps to keep the subMIC flybacks in DCM. Also, the duty cycle is constant for this mode.

The port voltage difference to current gain is now only dependent on port voltages. Given that the port voltage difference do not vary much, the output current will also not vary much. It will be near constant. The converter will act like the processed power is limited and saturated. This is the first measure taken to limit the power processed in the subMICs. However, if the port voltage difference increases, processed power can still scale with the port voltage difference. The next mode protects the converters from this extreme case.

The *Limit* Operation The *Sat* mode does not provide strong power limiting functions when the port voltages vary. The *Limit* mode acts as a hard power limit by turning off the converters when the port voltage difference is too high. This is possible when mismatch between a substring to the rest of the substrings is too high or a short occurs. When mismatches are too high, there are less benefit processing the power. The efficiency of the subMICs start to matter. It can be better to shut off the converter and let the by-pass diodes conduct. However, this condition is very unlikely to happen during normal operations. More analysis of this mode is done in later chapters.

Unlike all the other modes, the *Limit* mode is not symmetric between the primary side and secondary side operation. In the primary side operation, duty cycle is fixed to a very minimal duty cycle (D_{min}). This is to allow the start up of the system. Initially, the secondary side port needs to be charged up from zero volts so that at least one of the subMICs are out of the initial *Limit* mode. Using a very low duty cycle would be very inefficient. However, the only time the primary side will operate in *Limit* mode are at start up, secondary side shorts, or when the rest of the substrings are all generating too less of a power. Hence, the low efficiency is not of a concern.

3.4.2 Controller Blocks

The design of the controller IC is explain in this section. The IC is designed with common key components such as the TCA, comparator, and references that are used in all

other blocks in the system. All identical components follow the same specifications. Design of these blocks are shown in the Appendix.

Using this approach, the analog blocks can be used as simple building blocks and it is less prone to errors in design. The trade off of this design method is the inefficient use of die space and power consumption. Power consumption is reduce using power management controls to compensate for this disadvantage. The design are done with 5V devices in a CMOS 5V/1.8V process.

The controller IC functions can be classified into three large blocks by the purpose of use:

- Primary side functions : Controls the main control schemes
- Secondary side functions : Generates the secondary side voltage as PWM
- Housekeeping functions : Provides reference and power management to other blocks

Primary Side Function Blocks The primary side function blocks perform all the operation modes described in Section 3.4.1. First, the *main_blk* senses the port voltages and processes the port voltage differences. The outputs are connected to compensating functions, which is a portion of the gain K_p. All mode determinations are based on the compensated port voltage difference, except for the *Limit* mode. The main function of the *triwave_blk* is to generate a precision triangle waveforms at a fixed frequency. The triangle wave is used as a reference to generate PWM duty cycles and also serve as a reference to determine control modes. The *limit_blk* also compares port voltage differences, but only uses it to determine the *Limit* mode. The last block, PWM_blk, gathers the output signals of all other blocks to determine the output duty cycles. The overall structure of the primary side function blocks are shown in Figure 3.13.

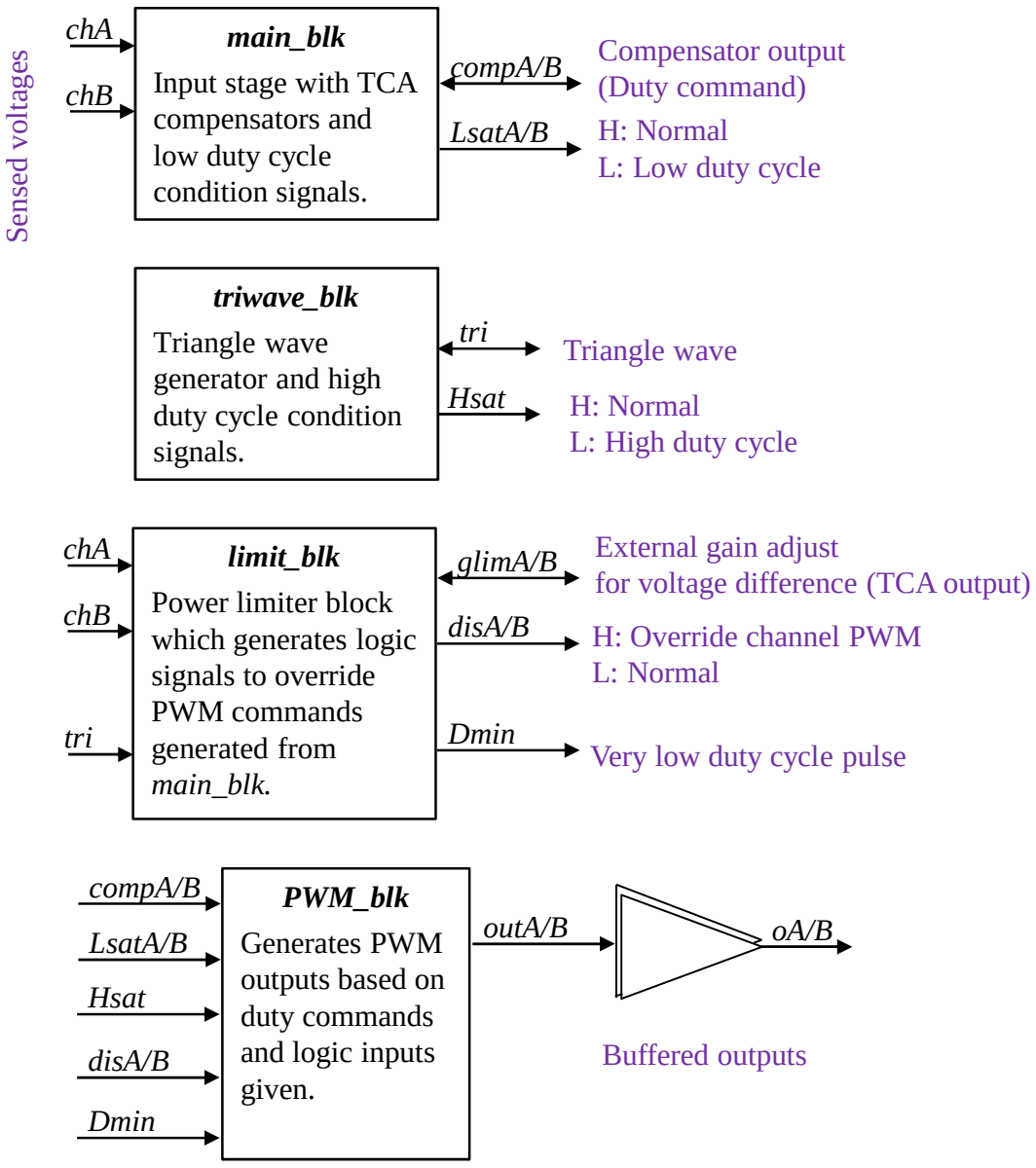


Figure 3.13: Structure of the primary side function blocks.

The inner structure of the *main_blk* is shown in Figure 3.14. It consists of a differential output TCA processing the port voltage differences (*chA* and *chB*), followed by compensating passives on *compA* and *compB* to form part of the gain $K_p(s)$. *compA* corresponds to the signal related to the primary side duty cycle, and *compB* to the secondary side. Sig-

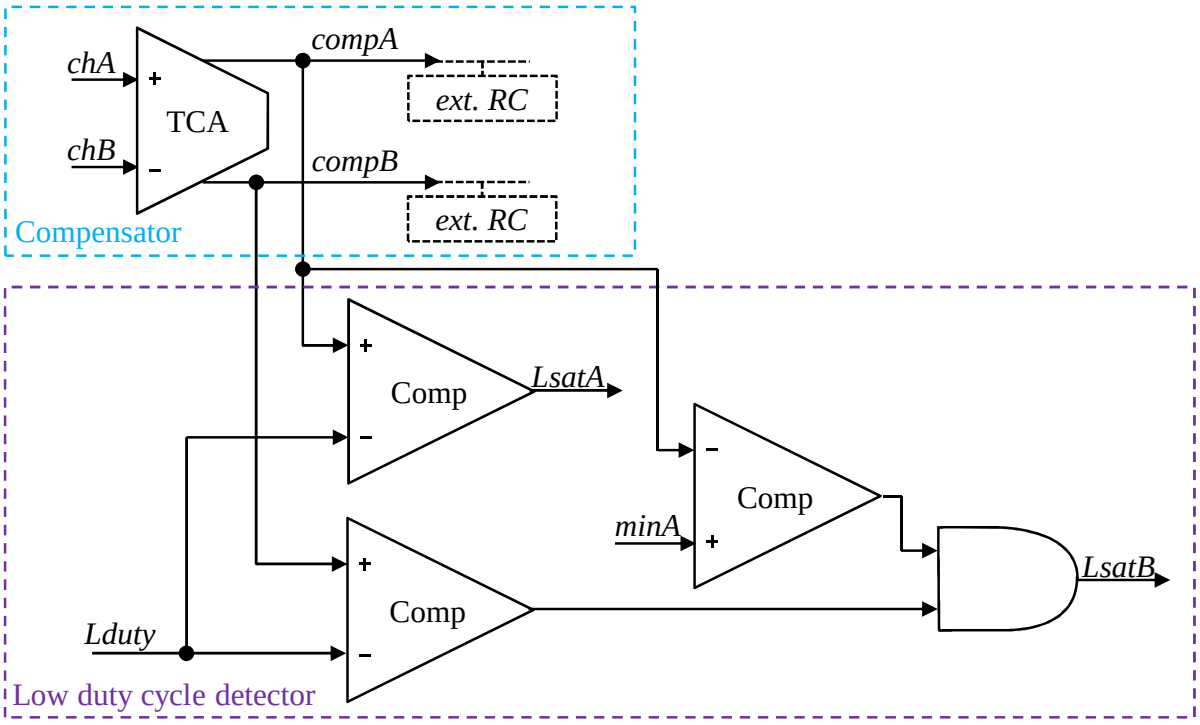


Figure 3.14: Structure of the *main_blk*.

nals *compA* and *compB* are routed out of the block as signals equivalent to a "duty cycle command".

These signals are also compared with a low duty cycle reference ($Lduty$) to determine if the duty cycle command is less than the minimum duty cycle allowed. If it is lower, $LsatA$ or $LsatB$ is triggered to operate the controller in the Off mode. Channel B also compares the duty cycle command to $minA$ so that duty cycle outputs of both channels are not operating at the same time. Figure 3.15 shows the signal relationships for the given reference signals.

The inner structure of the *triwave_blk* is shown in Figure 3.16. The *triwave_blk* consists of a triangle wave generator and a high duty cycle detector. The triangle wave generator uses a set of comparators that detect the peaks of a triangle wave at the *tri* output, toggling the precision constant current source and sink that charge and discharge the timing capacitor

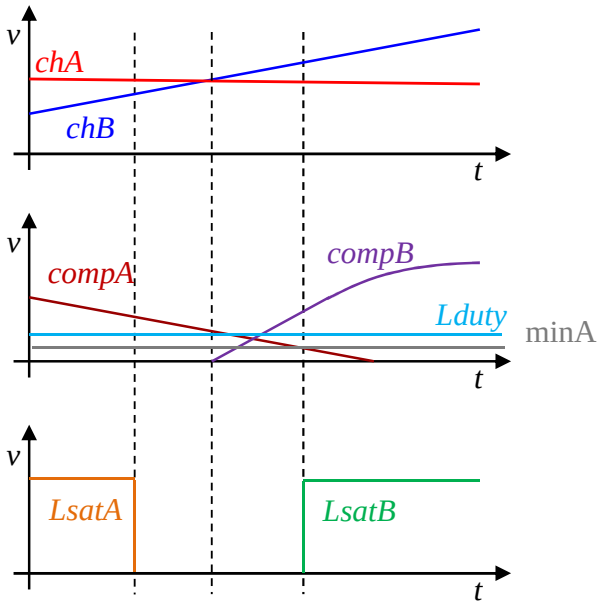


Figure 3.15: Signal relationship of the *main_blk* with changing port voltages.

on *tri*.

The high duty cycle detector generates a mask signal ($Hsat$) used to generate the saturated duty cycle for the *Sat* mode. It uses the *tri* signal as a reference to generate the mask signal. Then the signal provides a reference in time to let the PWM_blk know where to mask the PWM output for a saturated duty cycle. This automatically puts the controller in *Sat* mode when the *Linear* mode commands high duty cycles. Figure 3.17 shows the signal relationships for given reference signals.

The inner structure of the *limit_blk* is shown in Figure 3.18. The *limit_blk* consists of three blocks. First is a port voltage difference gain block with outputs $gainA$ and $gainB$. Compared to the similar block in the *main_blk*, this stage has a much lower gain to detect larger voltage differences.

The limit condition detectors compare $gainA$ and $gainB$ with the reference $Vlim$ to determine whether or not the controller should enter the *Limit* mode. If so, the corresponding flag, $disA$ or $disB$, is triggered.

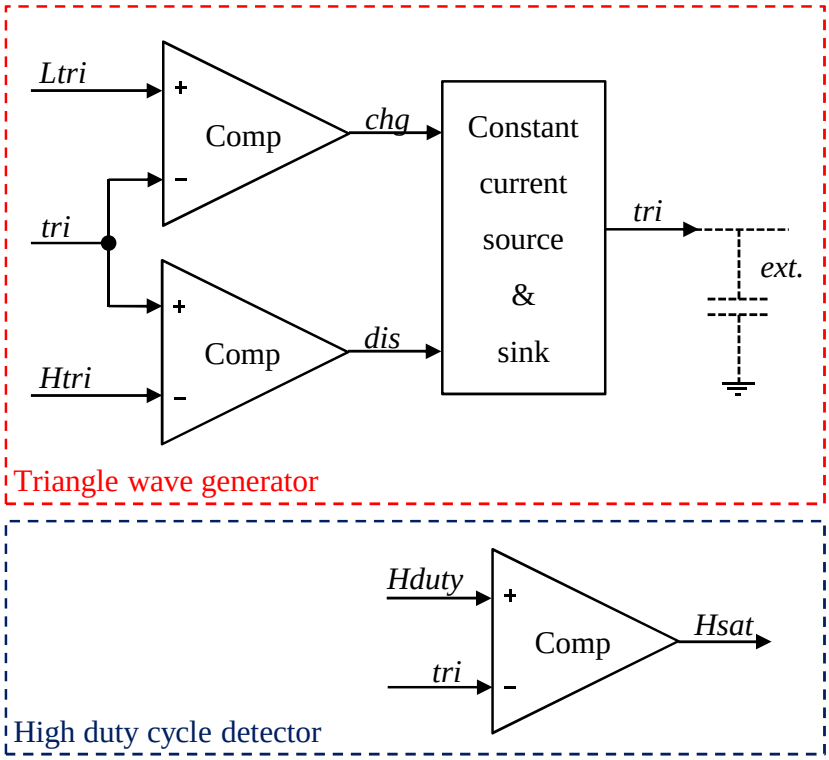


Figure 3.16: Structure of the *triwave_blk*.

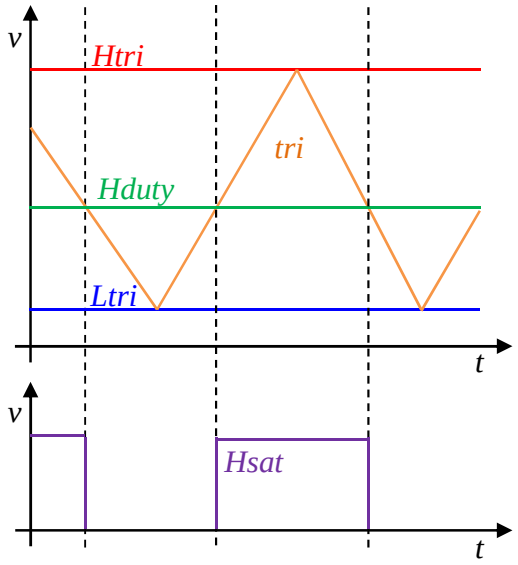


Figure 3.17: Signal relationship of the *triwave_blk* with changing port voltages.

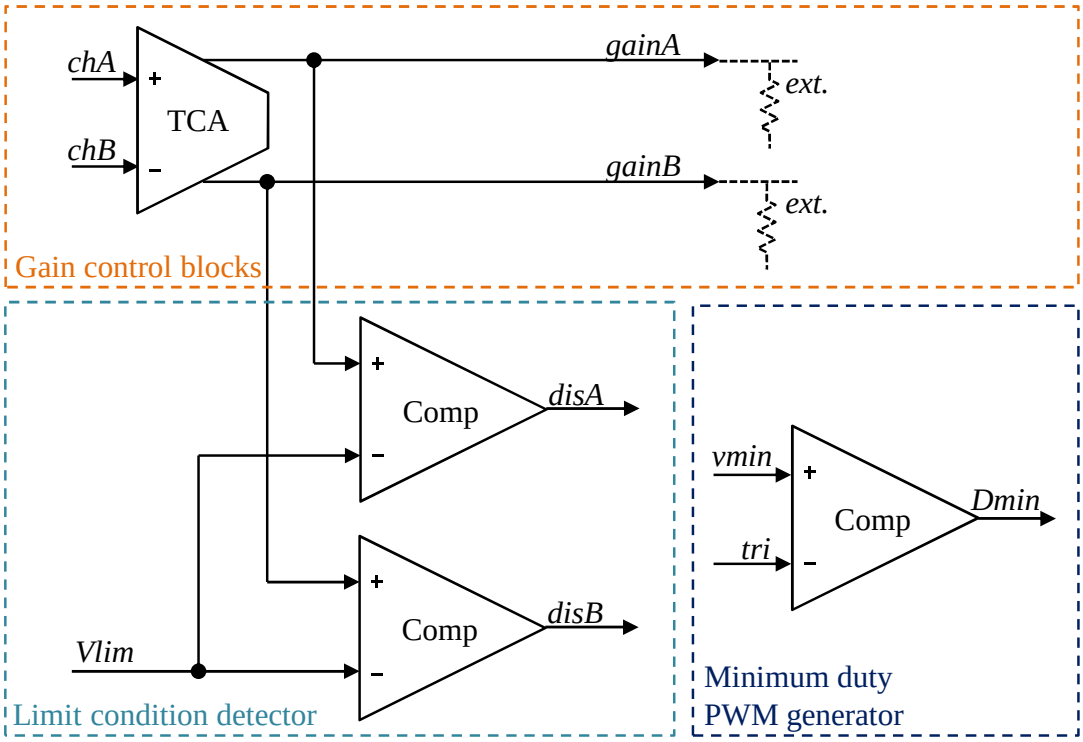


Figure 3.18: Structure of the *limit_blk*.

A very low duty cycle reference ($Dmin$), used at the primary side output in the *Limit* mode, is also generated in the block. Figure 3.19 shows the signal relationships for given reference signals.

The PWM_blk, which is part of the primary function, gathers all signal outputs from other blocks to determine the PWM output. The inner structure of the PWM_blk is shown in Figure 3.20. Note that there are two channels identical structures in the block. However, some input signals differ. The diagram combines the two channels. In Figure 3.20, the differences between the two channels are noted with a "/". The main input signals are $compA$ and $compB$, which are the duty cycle commands. Other signals that determine the modes are also used as inputs. The outputs of the block, $outA$ and $outB$, are the actual gate driving signals that drive the output buffers. It is easier to understand how this block functions through a logic truth table. It is show in Table 3.5. The function or purpose of the

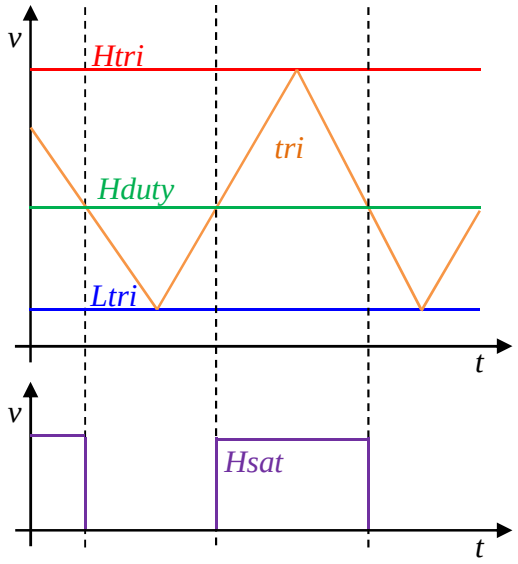


Figure 3.19: Signal relationship of the *limit_blk* with changing port voltages.

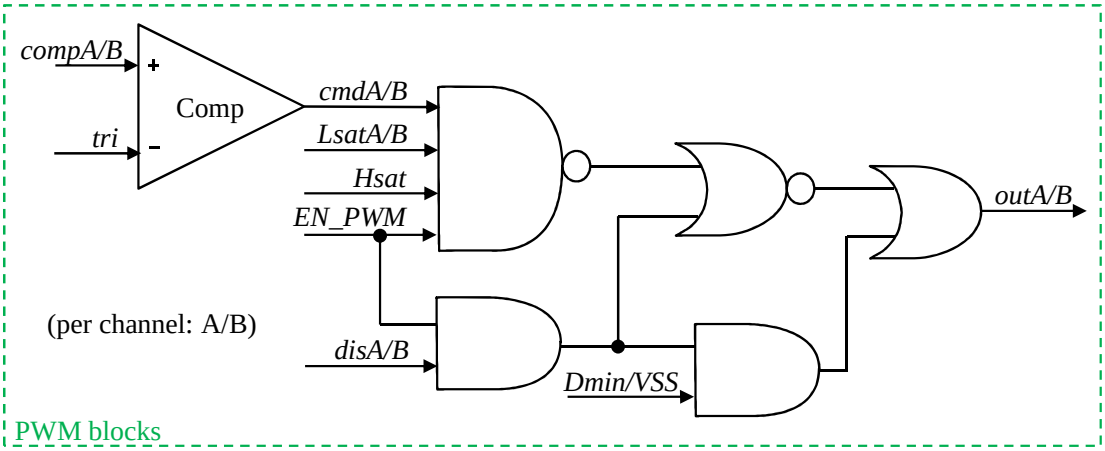


Figure 3.20: Structure of the PWM_blk.

logic states are explained in the comments of the table. The table includes all four modes of control, including the disabled state when EN_PWM is low. This signal corresponds to the ENp signal which explained in the housekeeping blocks in the following section.

Inputs A/B				*outA/B*	Comments
LsatA/B	***Hsat***	***EN_PWM***	***disA/B***		
H	H	H	L	*cmA or cmB*	Normal PWM
H	L	H	L	L	Cuts off duty above maximum (*D*=Saturated)
L	H	H	L	L	No duty since below minimum duty limit (*D*=0)
L	L	H	L	L	Combination of above conditions (abnormal)
x	x	H	H	*Dmin or* L*	*Channel A case: Fixed low duty cycle *Channel B case: Low output
x	x	L	x	L	Block is OFF

Table 3.5: Logic truth table of the combinational logic in PWM_blk.

Secondary Side Function Blocks When the IC is operated in the secondary side mode, only the *triwave_blk* and a portion of the output blocks are reused. All other blocks used in the primary functions are turned off to reduce power consumption. The structure is shown in Figure 3.21.

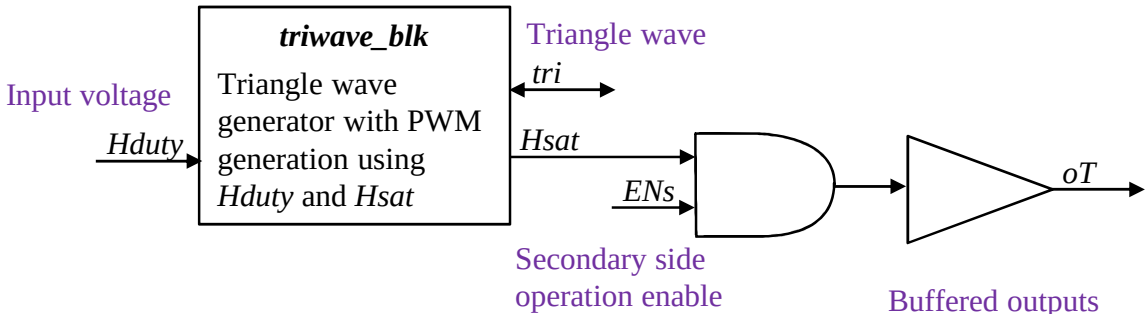


Figure 3.21: Structure of the secondary side function blocks.

Housekeeping Function Blocks

The housekeeping blocks consists mostly of references and the logic that control the power state of the references. The *bias_logic* block receives flags from other blocks and external signals. It determines which reference currents should be shut off in the ref_blk.

Also a experimental voltage reference block, bg_ref, is included. The structure is shown in Figure 3.22.

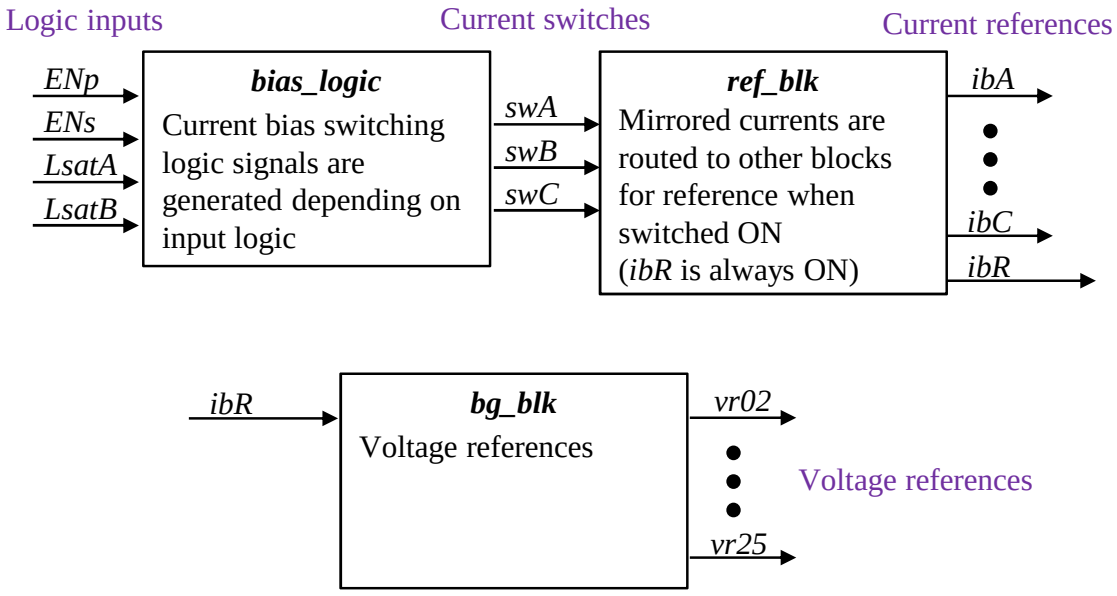


Figure 3.22: Structure of the power save and reference function blocks.

Table 3.6 shows the truth table for the combinational logic involved in the $bias\_logic$. ENp and ENs are external flag signals that determine the main mode of operation. $LsatA$ and $LsatB$ are the Off mode flags generated from the $main\_blk$. The output switch signals control the on/off of current references in ref_blk. Each of the blocks that corresponds to these switches are also shown in the Table 3.6.

Inputs				Outputs			Comments
ENp	***ENs***	***LsatA***	***LsatB***	***swA***	***swB***	***swC***	
H	H	x	x	H	H	H	All blocks always ON (Safe mode)
H	L	L	L	H	L	L	Only *main_blk* ON (quiescent, primary)
H	L	Other than L & L		H	H	H	All blocks ON
L	H	x	x	L	H	L	Only *triwave_blk* ON (quiescent, secondary)
L	L	x	x	L	L	L	All OFF
Switched current references are grouped as following : ***swA*** : *main_blk* ***swB*** : *triwave_blk* ***swC*** : *PWM_blk & limit_blk*							

Table 3.6: Logic truth table of the combinational logic in *bias_logic* block and the corresponding affected blocks explained.

3.4.3 Realization

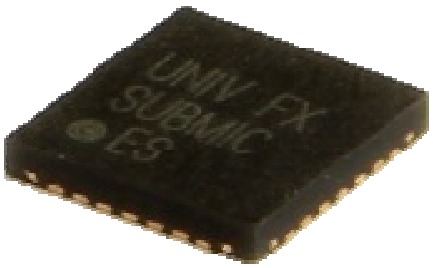


Figure 3.23: SubMIC controller IC packaged.

The layout of the IC is shown in Figure 3.24. The functional blocks are clustered in groups for easier layout. The core area of the layout is 0.7 mm by 0.7 mm. SubMIC controller IC is packaged in a QFN 28 pin package.

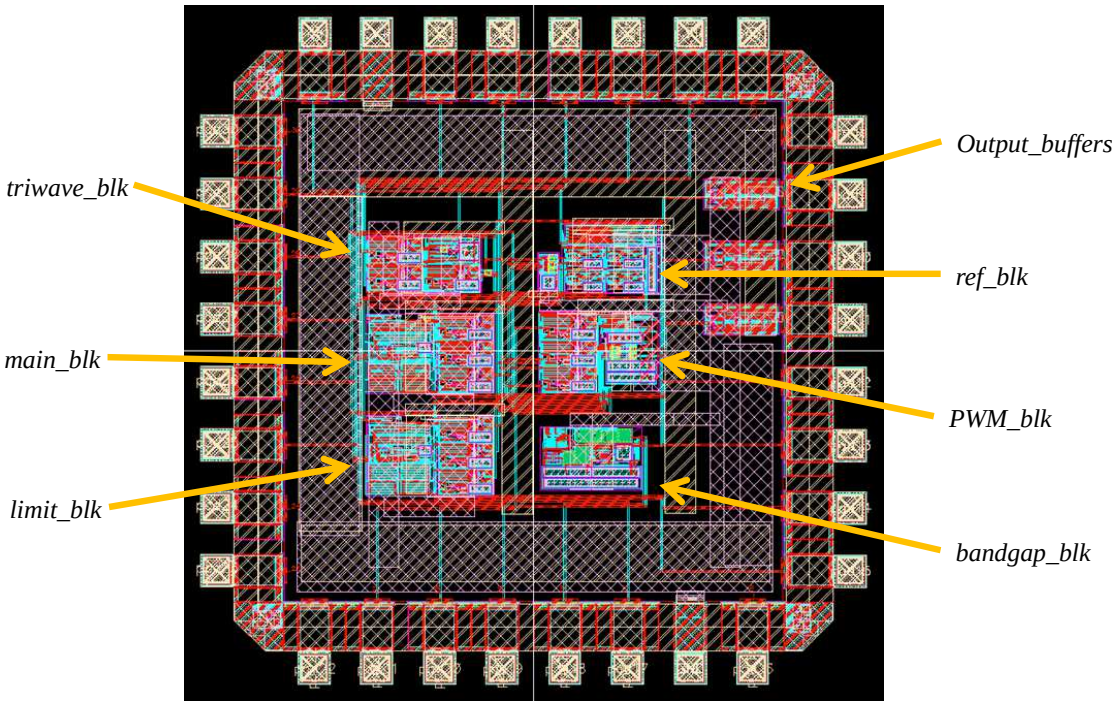


Figure 3.24: IC layout.

A post layout simulation is performed to validate the control mode transitions and confirm proper operation. It is shown in Figure 3.25. At the extreme input voltage differences,

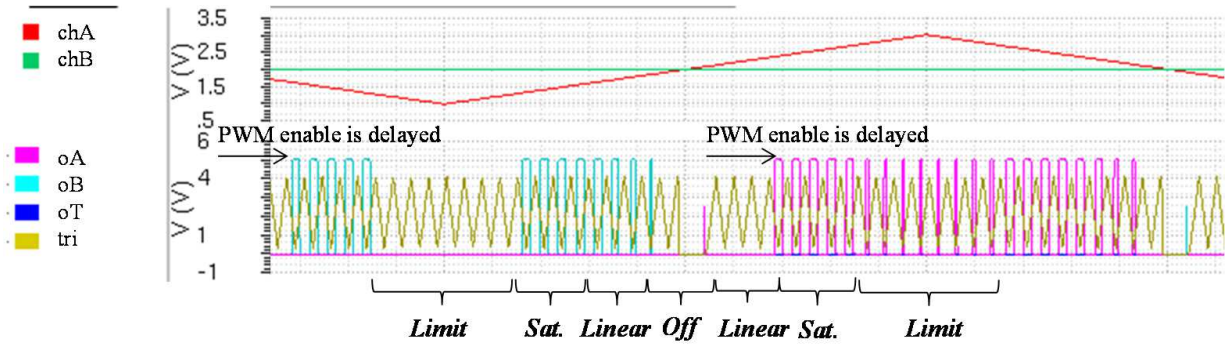


Figure 3.25: Post layout simulation validating the modes of control for primary operation. Top row shows the input voltage signals varying with time. Bottom row shows the triangle wave overlaid over the two PWM outputs.

control in *Limit* mode is verified by the zero duty cycle in the $chB >> chA$ case. For the

$chB << chA$ case, very low duty cycle is also verified. As the voltage difference between the input channels decrease, Sat mode is entered. This is confirmed by observing the constant 50% duty cycle. As the difference is closer to zero, linear change in duty cycle is observed, hence in $Linear$ mode. Finally, when the voltage difference is very close to zero, the PWM outputs are off as in the Off mode.

During the Off mode to $Linear$ mode transition, delay in mode change is observed. This is due to the intentional delay added to the transition. It ensures that the blocks that were turned off in the Off is fully turned on and stable before the PWM is enabled again. This prevents faulty outputs. In the background, a nice symmetric triangle wave is verified.

Next, the secondary side operation and the power save features are verified in Figure 3.26. The same simulation as in Figure 3.25 is used, but extended by switching ENp and ENs signals on/off.

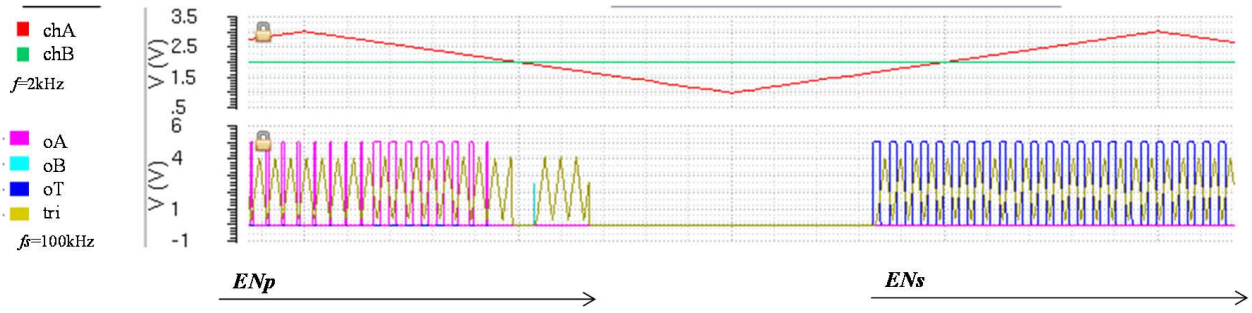


Figure 3.26: Post layout simulation validating the modes of control for secondary operation. Top row shows the transition from primary to secondary operation. Bottom row shows which set of blocks are on in each mode.

Observing the ENp high case, where the input voltage difference is also around zero, it is observed that swC is shut off. This corresponds to the shut off of the PWM_blk and the $limit\_blk$. When both enable signals are off, all blocks are shut off. Then, when ENs goes high, only swB signal is high. swB corresponds to the $triwave\_blk$ power. Also, the third output PWM is enabled when ENs is high. Also, the two primary output PWMs are

off during this state.

Simulations verify that the controller is behaving as expected in all operating modes.

3.5 Prototype Board

The prototype board consists of three subMICs in one PCB. The main PCB is a 2-layer 1 oz copper PCB. The planar magnetics are soldered on to the PCB. Each subMIC consists of a bi-directional flyback stage which includes a subMIC IC, LDO, and a digital isolator. A common secondary side circuit consists of a LDO and a subMIC IC which operates in the secondary side mode.

The board power rating is adjustable through the subMIC IC controls, but the full power rating is estimated to be at 60 W. The ELT20 core with the 442 winding configuration is selected for the prototype subMIC. This subMIC configuration shows 90% efficiency. The dimension of the board shown in Figure 3.27 is of 70 mm by 110 mm with 14 mm height with a volume of 113 cm^3. This prototype board is used throughout the experiments in the following chapters.

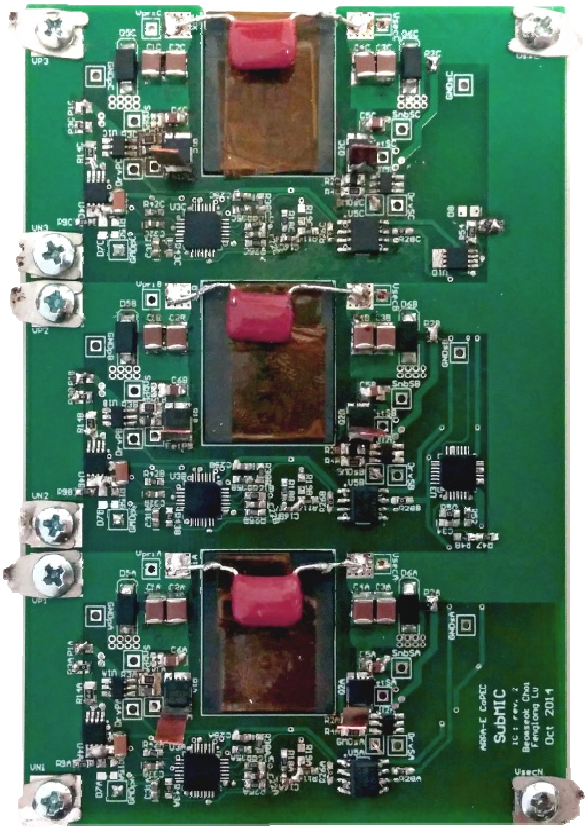


Figure 3.27: Prototype subMIC board with three subMICs.

Chapter 4

SubMIC Performance Evaluation

This chapter presents experimental results for the subMIC power stage and its components. First, the power stage is evaluated. The target efficiency of the bi-directional flyback is 90% throughout the load range. It is important that efficiency is maintained under light low conditions.

Next, the magnetics characteristics are measured, and the transformer performance in the flyback converter is evaluated. Relative efficiency differences between the magnetic designs are compared to find the optimal design. Then, the estimated losses are compared with measured results.

In the last portion of this chapter, performance of the controller IC is evaluated.

4.1 Power Stage Efficiency

First, efficiency of the flyback converter is evaluated. The prototype subMICs are designed to operate at switching frequency of 100 kHz and an estimated transformer magnetizing inductance of 7.3 uH. For the measurements, the output of a single converter is fixed to 12.5 V. Then, the input voltage is increased while the converter is operated in closed-loop. The converter controls are set to have a minimum duty cycle of 15% and maximum of 48%. With this setup, the duty cycle saturates around 25 W of power. For the comparison, ELT22

and ELT20 cores with the 442 winding setup are used. Results are shown in Figure 4.1.

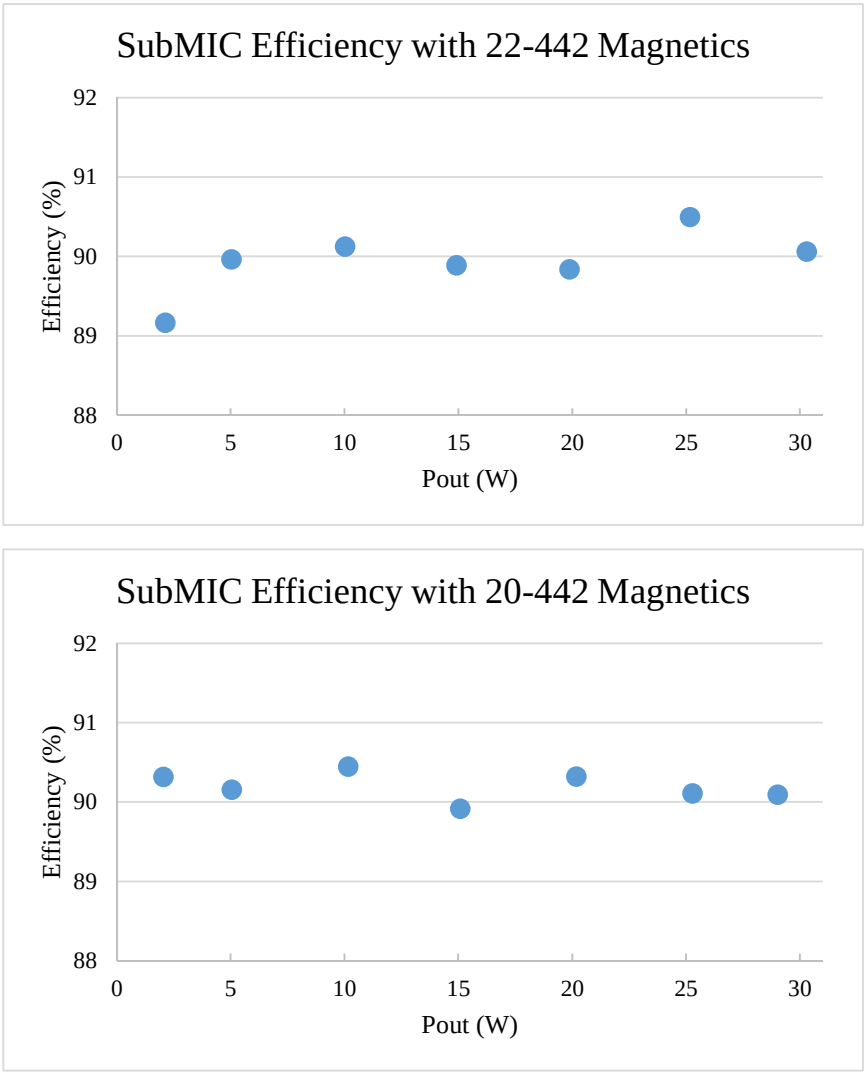


Figure 4.1: Measured subMIC power stage efficiency with the 22-442 magnetics (top) and the 20-442 (bottom).

From the results, both designs shows efficiency around 90% throughout the load range, down to 5 W. The efficiency is maintained even down to 2 W for the 20-442 design.

It can be concluded that the power stage demonstrates the target 90 % efficiency.

4.2 Evaluation of Magnetics Designs

Total of six different magnetic designs were manufactured for evaluation. The inductances of the designs were matched to be around 7.3 uH. The measured inductances of the designs are shown in Table 4.1.

20 size core	L_{Pri}	L_{Pleak}	L_{Sec}	L_{Sleak}	*Airgap*
20-55 (a)	7.58 uH	122 nH	7.82 uH	123 nH	5 mil
20-424 (b)	7.36 uH	90 nH	7.55 uH	100 nH	3 mil
20-442 (c)	7.26 uH	76 nH	7.42 uH	70 nH	3 mil

22 size core	L_{Pri}	L_{Pleak}	L_{Sec}	L_{Sleak}	*Airgap*
22-55 (a)	7.50 uH	90 nH	7.76 uH	112 nH	6 mil
22-424 (b)	7.42 uH	72 nH	7.60 uH	94 nH	3.5 mil
22-442 (c)	7.33 uH	47 nH	7.45 uH	49 nH	3.5 mil

* L_{pri} and L_{sec} includes leakage

Table 4.1: Measured inductances.

Comparing the results between the two cores, the 20 size core shows much larger leakage inductance. Comparing the windings, the 55 configuration shows 20% more leakage inductance than the 4 turns windings. Between 442 and 424 windings, the 442 showed much less leakage inductance. However, the table does not compare the parasitic capacitances. Airgap also differs between cores. Since the winding turn counts are so low, a step from 4 to 5 turns increases the required airgap by almost two.

4.2.1 Efficiency Measurements with Planar Magnetics

It is difficult to measure only the losses from the magnetics. Insetad, the converter efficiencies are compared in relative manner to evaluate the magnetics performance. Also,

the efficiencies estimated from the loss model are compared. Results are shown in Figure 4.2.

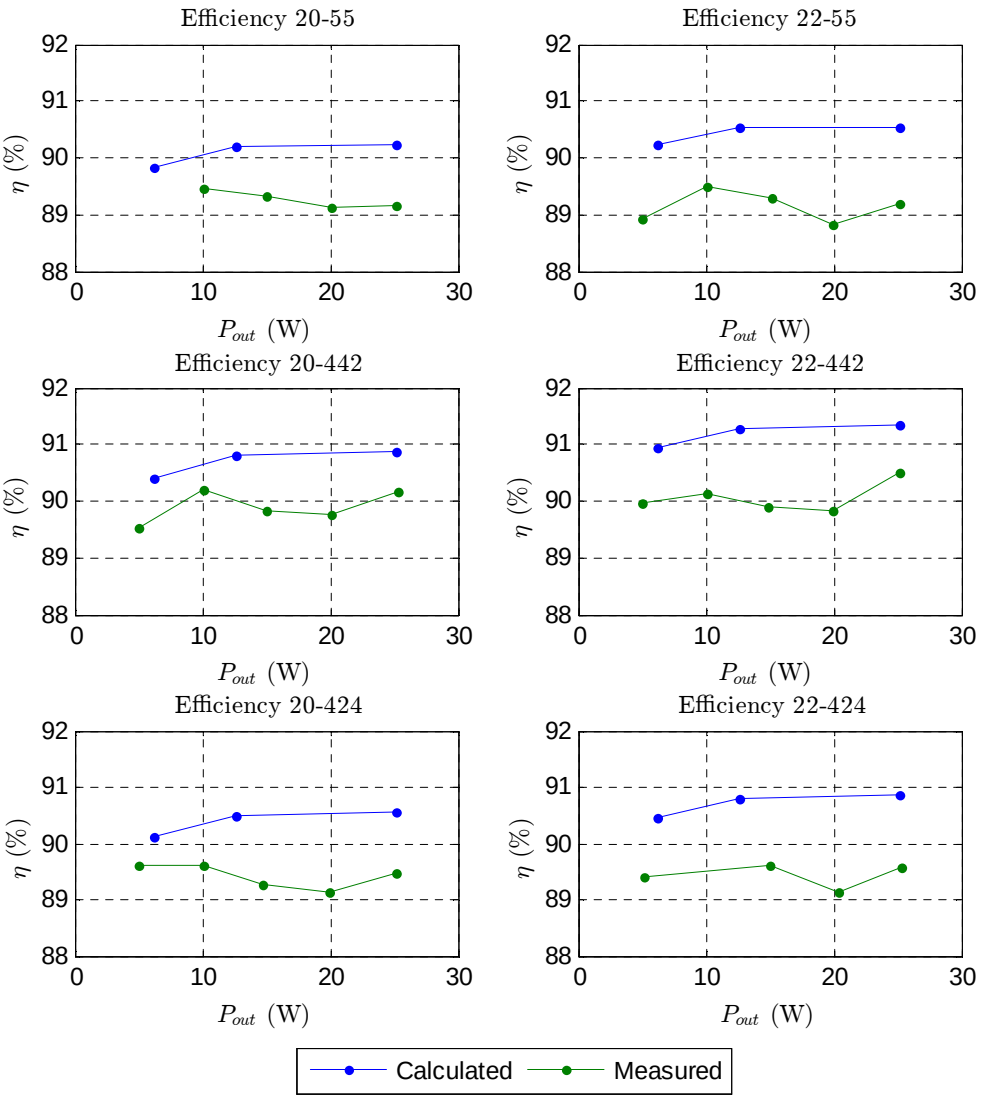


Figure 4.2: Converter efficiency comparison for different magnetics designs.

First, measured efficiencies are evaluated. Between the two core sizes, there is not much noticeable difference in efficiency. Comparing between the different winding designs, the 20-442 design shows the best efficiency, while 20-55 and 2-424 shows similar efficiencies.

Now, comparing the estimated efficiencies to the measurements, an offset in efficiency

is observed. Ratio wise, the efficiency estimations follow the measured efficiency well. This is true between the winding design variations. However, the estimation and measurements do not agree well for core variations.

For better insight of the offset present between the estimation and measured losses, a loss budget analysis is performed using the estimation results. It is shown in Figure 4.3.

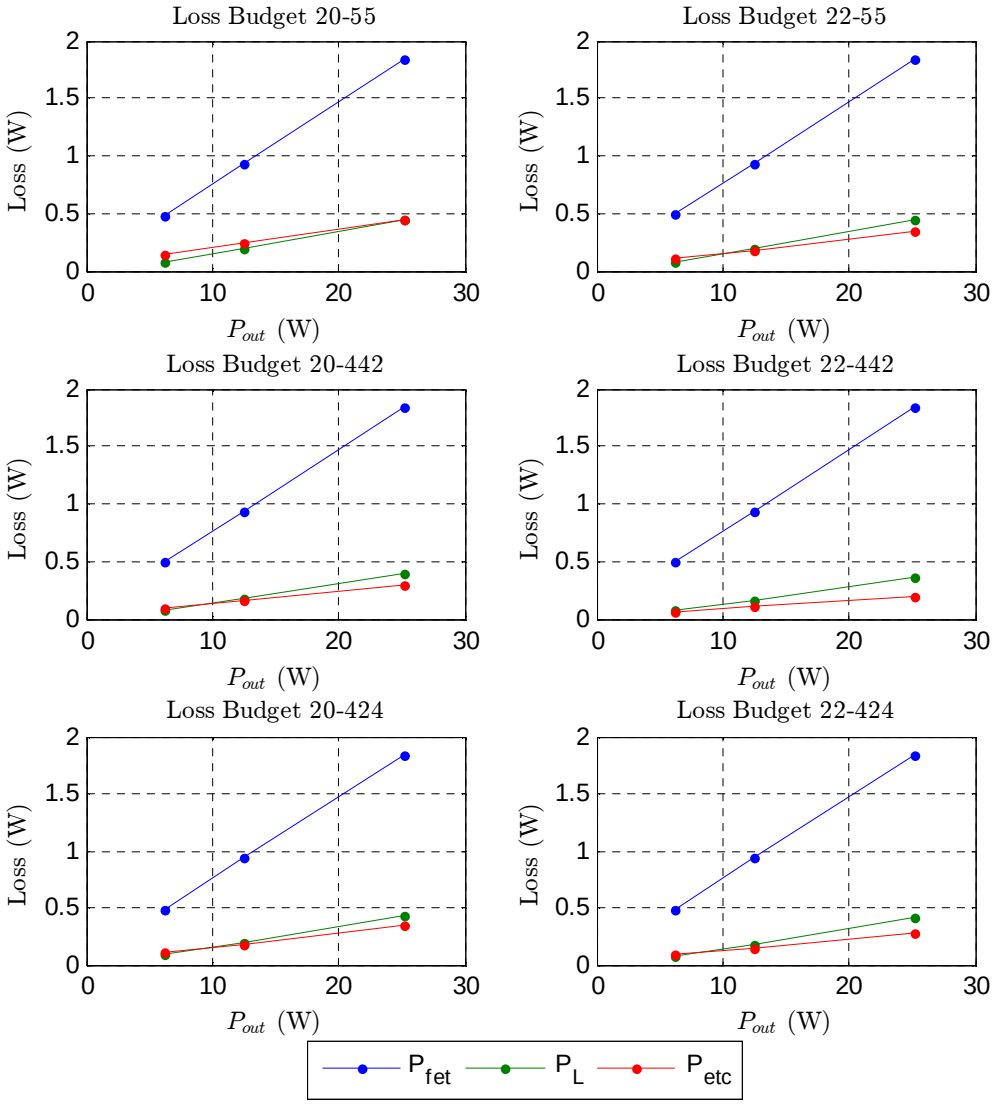


Figure 4.3: Converter loss budget from the estimated losses where loss occurring on the MOSFET (P_{fet}), the inductor (P_L), and other losses (P_{etc}) are shown.

Analyzing the loss budget, the loss occurring at the MOSFETs dominate the loss. This is mostly due to the body diode conduction loss. The body diode conduction loss accounts for more than half of the total efficiency drop. However, the forward voltage drop of the body diode varies with temperature, causing significant variances in the measurement. Also, the variations in diode conduction losses will look like offsets in the efficiency versus load curve. Therefore, the magnetic loss estimations were good at estimating relative performance between winding designs. However, the performance estimation between the cores did not predict well.

Next, loss budget of the magnetic losses are analyzed. The loss budget gives a better idea of where the estimation errors could occur. Figure 4.4 shows the results.

Comparing the loss budget between the two cores, differences in leakage inductance related losses can be observed. Results suggest there could be errors in measuring the leakage inductances. However, without further experiments, the cause of the error can not be sure.

Finally, loss from the airgap fringing flux is evaluated. In Section 3.3.2, FEMM simulation has showed that the AC copper loss of a 125 mil thick board is double the loss of a 93 mil board. The board thickness of the planar winding is of 110 mil. This gives the winding about 58 mil distance from the airgap. Experiment on loss versus distance from the airgap is perform by lifting the windings closer to the airgap in incremental steps. Results are shown in 4.5.

Results show that converter efficiency drops throughout the load range as the distance from the airgap decreases. Comparing the two extreme cases, 18 and 58 mil distances, 1% difference in converter efficiency is observed. Comparing the 58 mil and 48 mil case, little difference in loss is observed. Hence, further increase of the distance from the airgap would not increase performance much more. This agrees with the estimate from FEMM analysis.

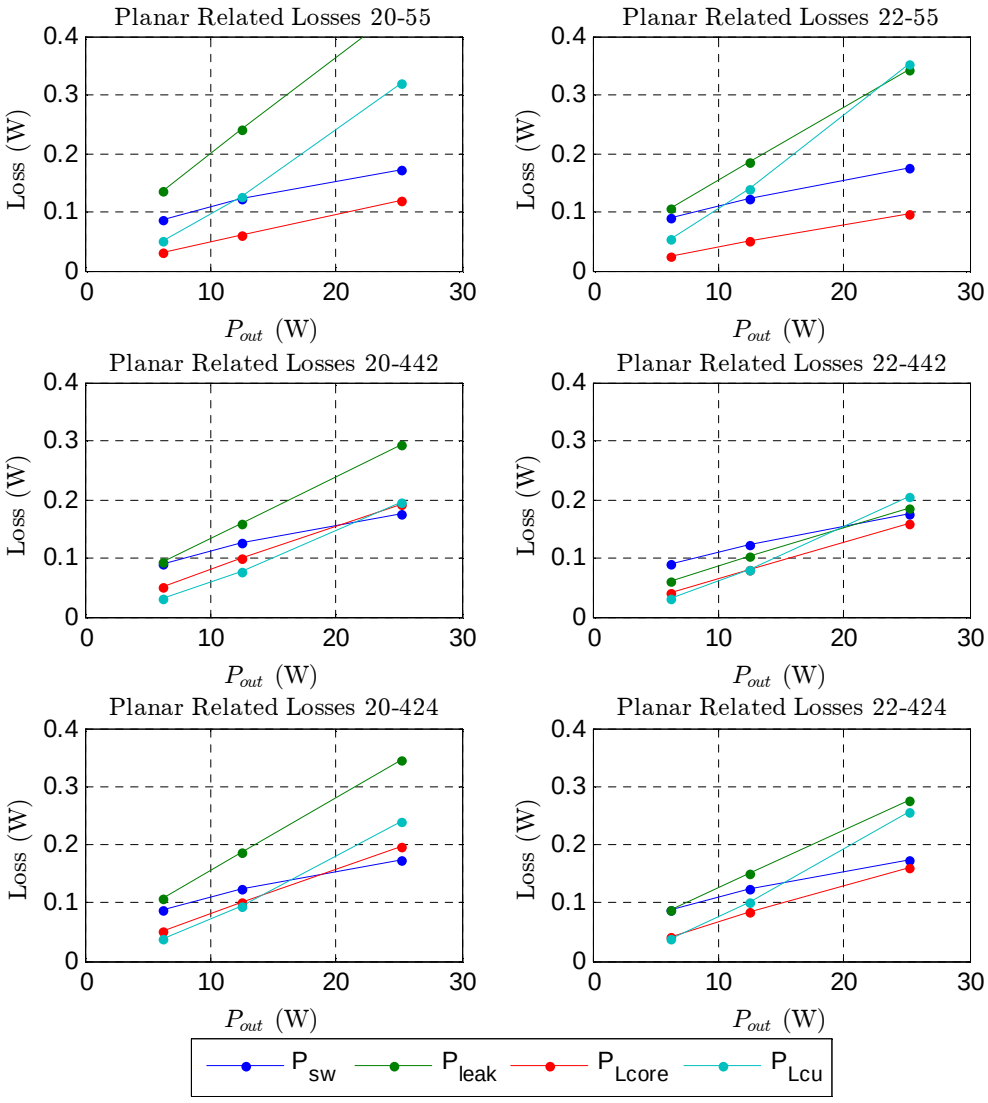


Figure 4.4: Magnetics loss budget from the estimated losses.

4.3 Controller IC Validation

In this section, the functions of the controller IC is validated. The focus of the validation is to make sure that there are no functional flaws. Performance and matching of the components were evaluated, but not presented in this section. The test board for validation is shown in Figure 4.6. The board is design to test three ICs at the same time.

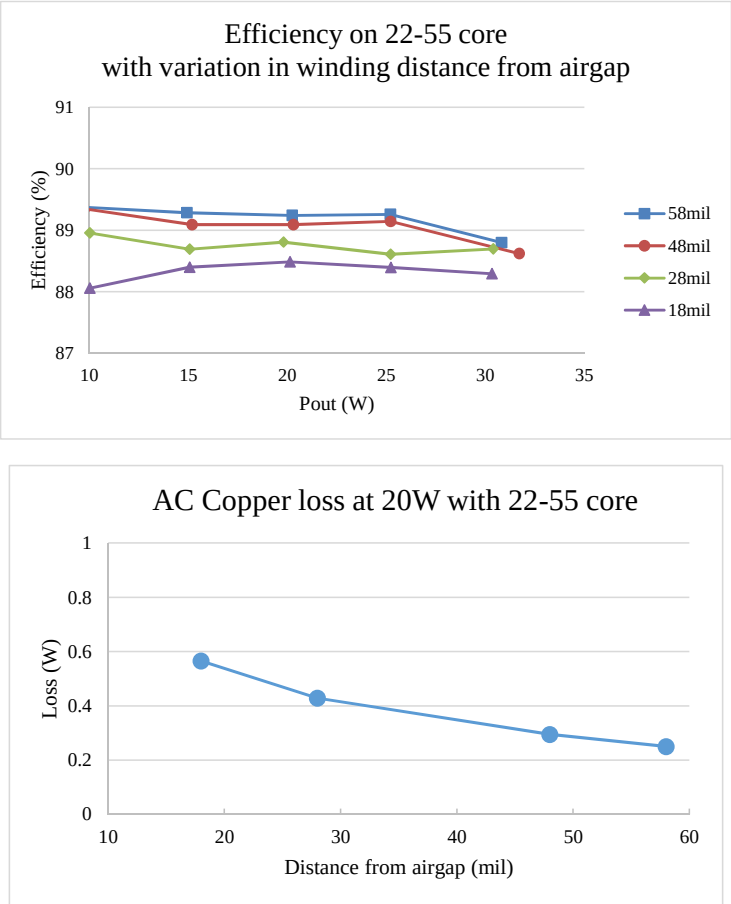


Figure 4.5: Converter efficiency (top) and AC copper loss estimate (bottom) compared with varying distance from the airgap.

4.3.1 Block Tests

First the most critical triangle wave generating function is evaluated. A symmetric constant slope should be present in the triangle wave. Figure 4.7 shows the evaluation results for a triangle wave at about 100 kHz with peaks at 1 V and 4 V. It is verified that the slopes are near constant and symmetric.

Next, TCA outputs are evaluated. Test is configured so that the outputs can saturate with the swept input voltage range. *chA* signal is ramped up and down crossing a constant *chB* voltage. The results in Figure 4.8 shows the resulting outputs. It shows that a linear

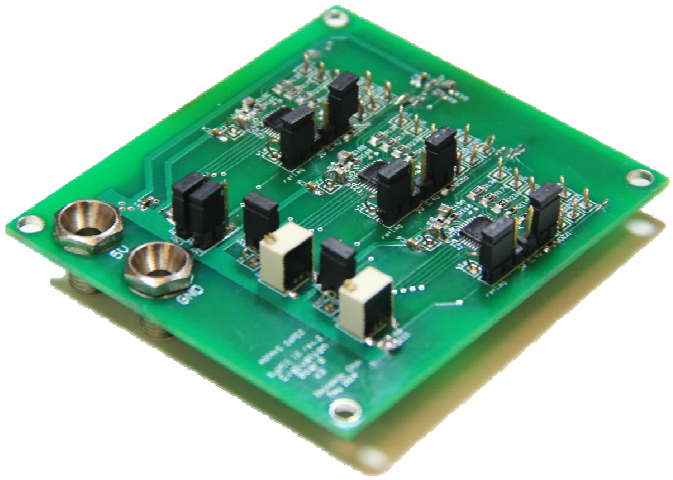


Figure 4.6: SubMIC IC evaluation board.

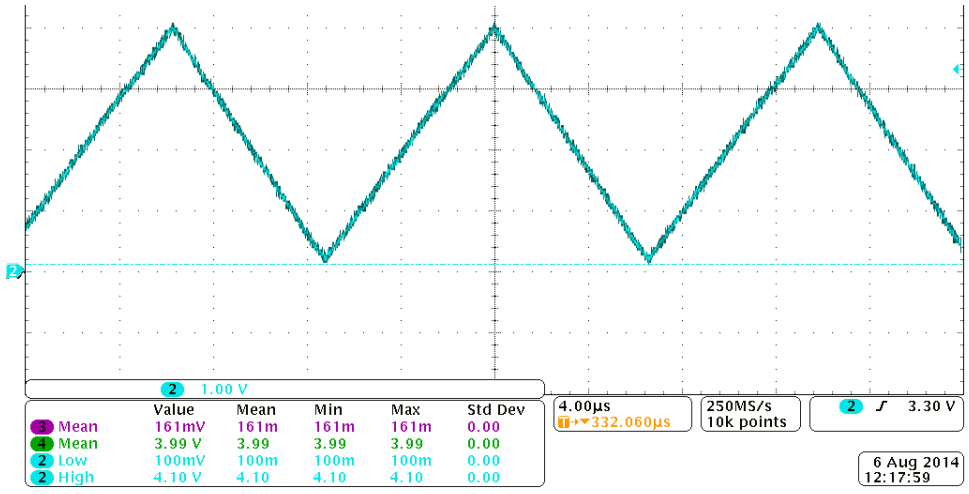


Figure 4.7: SubMIC triangle wave.

output can be expected up to 4.5 V. The TCAs will be used in the 1-4 V range, which is in the linear range.

Another key function to validate is the power managing functions. The power managing function controls the on/off other functional blocks. This causes transition times and adds

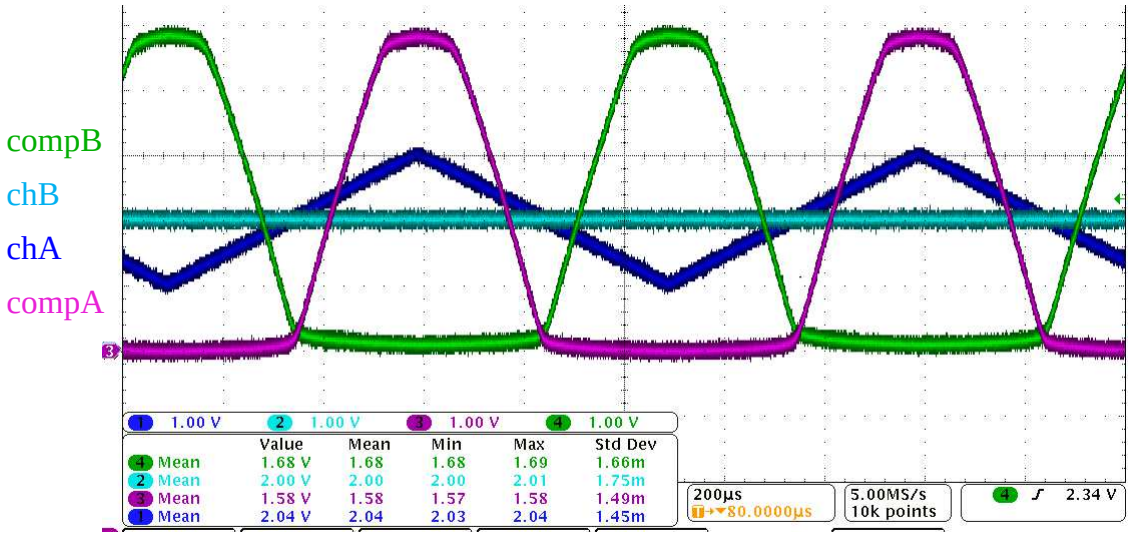


Figure 4.8: SubMIC TCA outputs.

complexity to the system. Input voltage is swept as in the TCA validation. Results are shown in Figure 4.9.

The most critical transition is between the Off mode and *Linear* mode. In the Off mode, most of the blocks are turned off. This can cause incorrect operation if the on/off transitions are not done correctly.

First, the Off mode operation is verified in the results. When the input voltage difference is near zero, it can be observed that the triangle wave is off. Hence, in Off mode. When the voltage difference is sufficient, the triangle wave is turned back on. The delayed output of the PWM signals is also observed and verified. This is intended so that all other blocks are operating at steady state before any PWM outputs are enabled. This is roughly a 20 μs delay.

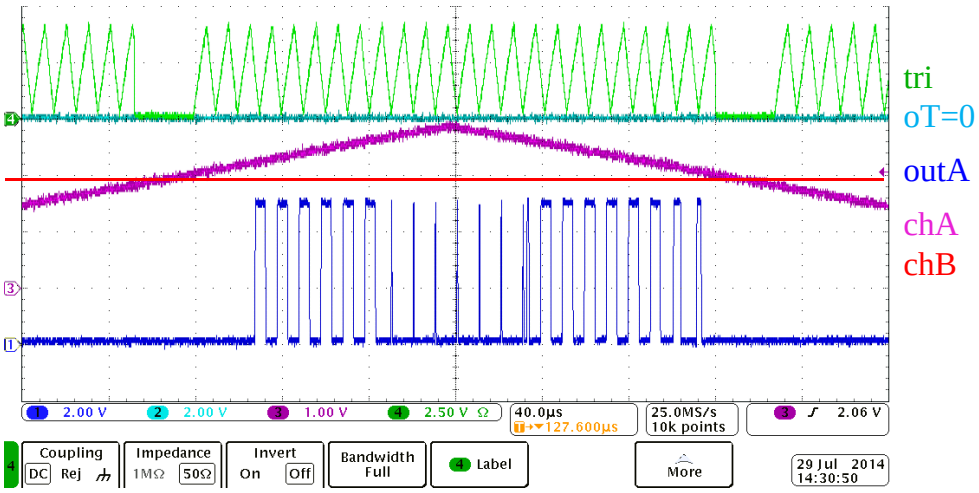


Figure 4.9: Input voltage sweep to validate power managing functions.

4.3.2 System Tests

System tests are performed to verify that the controller functions smoothly throughout all control modes. This evaluation is an attempt to replicate the post-layout simulation performed in the design process as in Figure 3.25. The primary side mode is set by ENp=1 and ENs=0. Due to the oscilloscope resolution required to verify the duty cycles, a collage is made of the oscilloscope measurement results. Results are shown in Figure 4.10. The waveforms look identical to the behavior in the post-layout simulation.

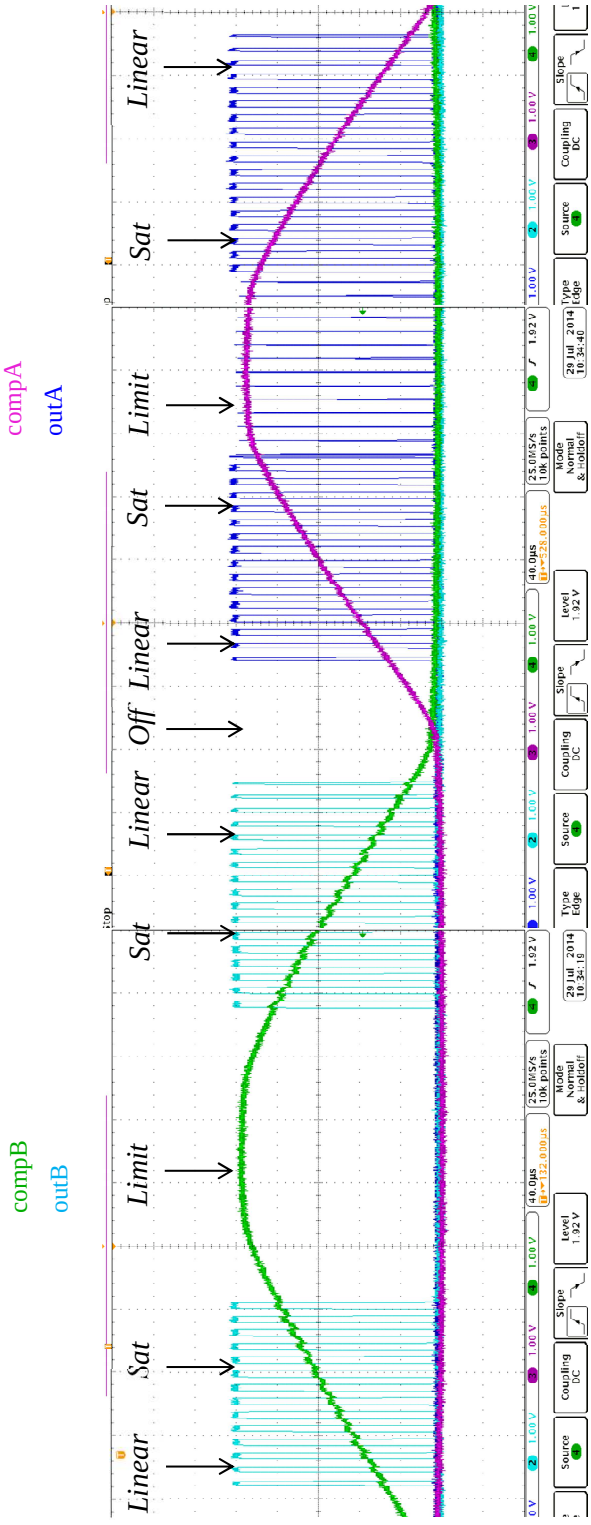


Figure 4.10: Primary side operation verification.

Next, the secondary side operation is evaluated. The secondary side mode is set by ENp=0 and ENs=1. The function is verified by comparing the reference voltage on $Hduty$ to the tri signal. It is confirmed that the PWM output works as expected. The result is shown in 4.11. The slight skew seen in the PWM is from the 10 nF load connected to the output. In the prototype, the output of the PWM will see a much smaller load.

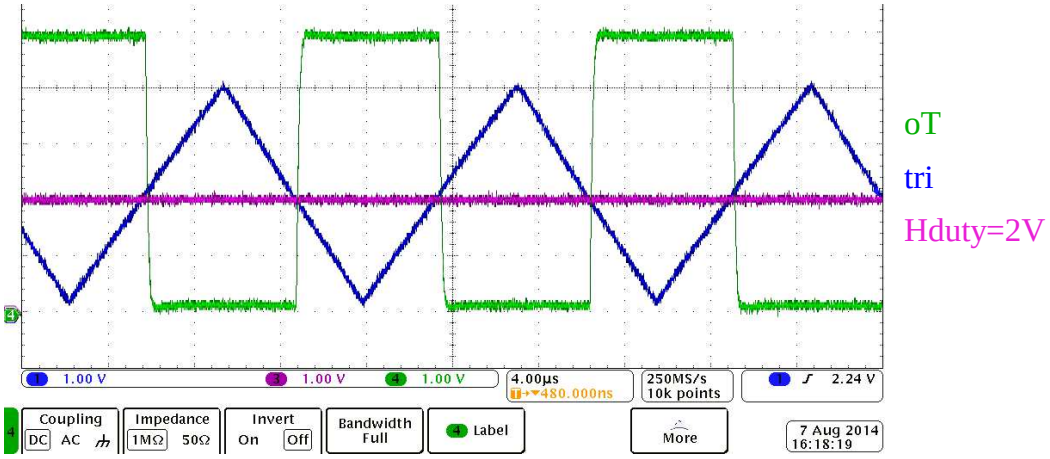


Figure 4.11: Secondary side operation verification.

4.3.3 Quiescent Power Consumption

One benefit of the DPP system is that there is no insertion loss. If the subMICs consume too much power at idle, the subMICs would contribute to loss even under no power mismatch in the PV system. Minimizing the power consumption at idle was one of the key specifications for subMIC IC design. The IC shuts down most of its internal functions when there are no mismatch present.

The power consumption of the prototype board is analyzed. The power consumption includes the three primary side subMIC circuits, and the common secondary side circuit. A 12 V port voltage is assumed for all four ports. The secondary side subMIC IC is assumed

to be operating the triangle wave at 1 MHz. All resistor based voltage dividers, isolators and LDOs are also considered. Table 4.2 shows the results. Results show that the board

		V	mA	mW
Primary Side (1 per SubMIC) fs=100kHz	SubMIC	5	0.80	3.5
	Gate Driver	12	0.10	1.2
	Isolator	5	2.30	11.5
	Resistors	5	0.20	1.0
	LDO	5	0.02	0.1
	Sum			**17.3**
Secondary Side (1 per 3 SubMIC) PWM frequency =1MHz	SubMIC	5	1.20	6.0
	Gate Driver	12	0.10	1.2
	Isolator	5	2.80	14.0
	Resistors	5	0.10	0.5
	LDO	5	0.02	0.1
	Sum			**21.8**
Total (Single SubMIC)				**39.1**
Total (All 3 SubMICs)				**73.7**

Table 4.2: Quiescent power consumption of the prototype subMIC board.

consumes under 100 mW of power. If the PV panels are producing 100 W, this would be equivalent to only 0.1% of loss.

It can be concluded that the subMIC controller IC is functioning as expected and ready for use in the subMIC prototype.

Chapter 5

System Performance Evaluation

In this chapter, performance of the DPP subMIC system is evaluated. The prototype subMIC board with three subMICs is used in the evaluation. Both indoor and outdoor experiments are performed. The indoor experiment provides a more controlled environment where the PV substrings can be biased to emulate various power settings. On the other hand, the outdoor experiments provide a more realistic environment for the PV system.

Throughout the experiments, the prototype subMIC board designed in 3.5 is used. It is connected to the three substrings of a 175 W PV panel. The isolated bus is connected in parallel to each of the subMIC modules. SubMICs are rated at 60 W, but can be power limited to operate at lower power ratings. A DC load is connected to the PV module output to emulate the inverter operation.

Performance comparison is done using the system efficiency. System efficiency is a measure comparing the energy captured from the PV system versus the maximum possible energy capture when all PV substrings are operating at MPP (E_{ideal}). The following equation shows the definition.

$$\eta_{subMIC} = \frac{E_{subMIC}}{E_{ideal}} = \frac{P_{subMIC}}{P_{ideal}} \tag{5.1}$$

$$\eta_{conv} = \frac{E_{conv}}{E_{ideal}} = \frac{P_{conv}}{P_{ideal}} \tag{5.2}$$

System efficiency is compared between the conventional structure as in Figure 1.5 (η_{conv})

and the subMIC-enhanced module (η_{subMIC}).

5.1 Bench Experiments

The main focus of the indoor experiments is to evaluate the system performance under a controlled environment. Indoor experiments are performed at a module level with three substrings tied to the subMIC board. The PV substrings are biased with current sources that emulate various levels of insolation. Figure 5.1 shows how the bias would equivalently look like if biased at the string level.

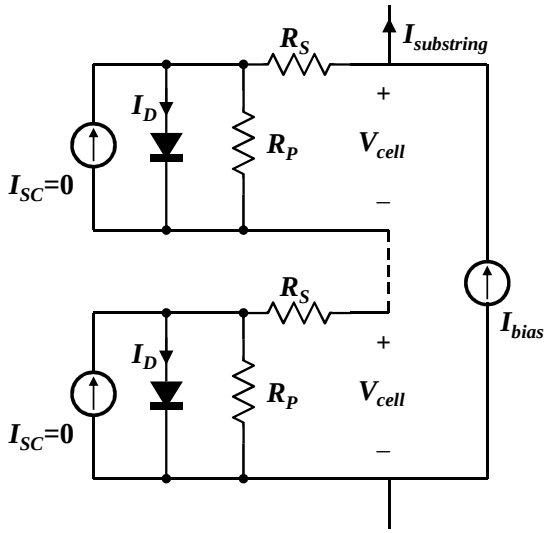


Figure 5.1: Current biasing a PV substring.

Compared to the case where I_{sc} would be sourcing current under actual insolation, an externally current biased string would show somewhat different characteristics. The dominant difference would be from the voltage drop on the series resistance R_s. Current flow on R_S is in the opposite direction. Consequently, the indoor experiment will show higher MPP with higher power. The indoor experimental environment could be improved by other methods that emulate the PV characteristic using power converters or circuits [33–35]. However, R_S is not critically large and would not have a large impact on the performance

comparison of the systems. Instead, outdoor performance experiments are performed, with results reported in the following sections, to validate the performance under true sunlight.

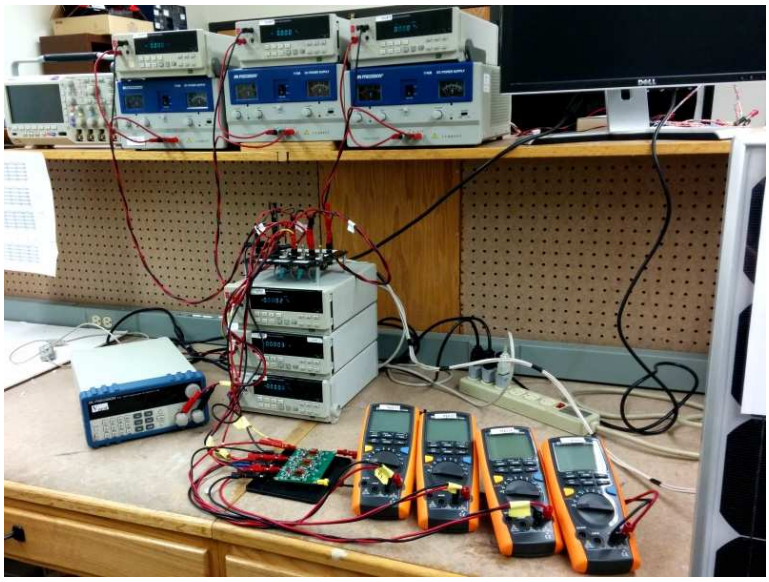


Figure 5.2: Indoor experiment setup.

5.1.1 Distributed Mismatch at Full Power Rated subMICs

This experiment evaluates the case where mismatch is distributed among the three substrings. The power variation are determined by the current biases which are shown in Table 5.1. The mean current is 3 A.

	Substring		
Power variations (%)	1	2	3
25 %	3.375 A	3 A	2.625 A
50 %	3.75 A	3 A	2.25 A

Table 5.1: Distributed mismatch bias currents.

The PV sweep results are shown in Figure 5.3. The ideal PV curve of both mismatch cases are identical, since the mean bias current are the same. In both cases, the PV curve of

the subMICs follows the ideal curve very closely. The V_{MPP} of the subMIC case are also very close, with less than a volt difference. On the other hand, the conventional case shows much lower peak power. Also, as mismatch increases, the V_{MPP} of the conventional PV module deviates to a higher voltage. When performing MPPT at the system level, the conventional system would show multiple maxima, depending on conducting states of the bypass diodes. The wide V_{MPP} range with multiple maxima must be considered in the design of the inverter MPPT algorithm, as in the design of the inverter itself, to accommodate a wider range of input voltages. In contrast, the subMIC-enhanced PV module shows that it not only has a single maximum, but that the MPP voltage is very close to the ideal V_{MPP}. These features can translate into advantages at the system level, including potentials for improved inverter efficiency and reduced cost.

Next, the system efficiencies are compared in Table 5.2. The subMICs keep the system level loss below 2% of the ideal case even at 50% mismatch. The conventional case shows nearly 20% system loss at 50% mismatch.

Efficiency (%)	SubMICs	Conventional
25 % mismatch	99.4 %	93.7 %
50 % mismatch	98.3 %	82.2 %

Table 5.2: System efficiencies for distributed mismatch.

5.1.2 Single Substring Mismatch with Power Limited SubMICs

Next, the system is evaluated with power limited subMICs. The subMIC power is limited to 20 W, which is about 30% of the substring PV power rating. The saturated control current would be approximately 1.6 A.

Substring mismatch is now performed on one substring by decreasing its power incrementally. A single substring mismatch scenario is used to help force at least one of the subMIC stages to enter the power limit mode. Also, it is convenient to observe the outcomes.

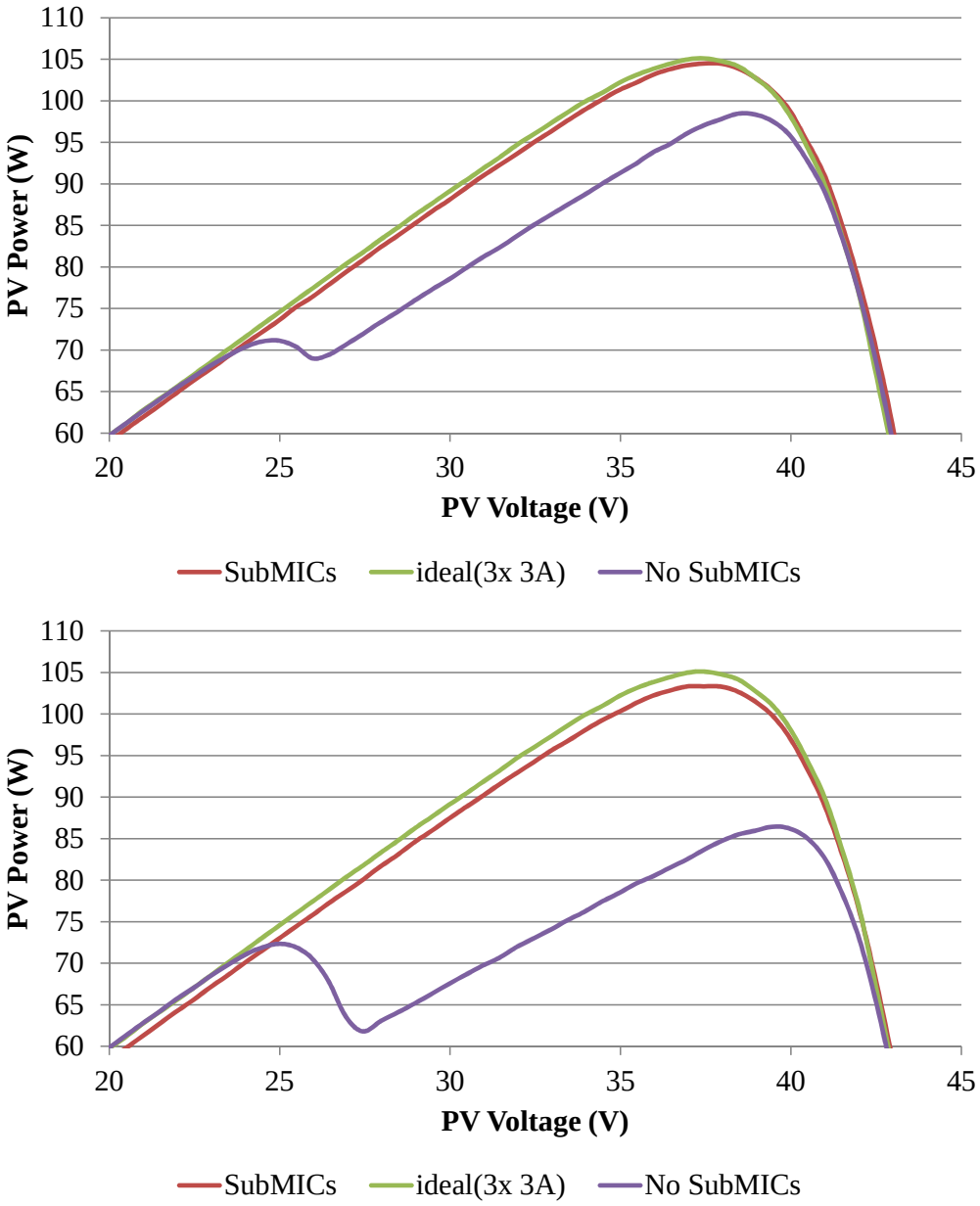


Figure 5.3: PV sweep of distributed 25% mismatch (top) and 50% mismatch (bottom).

In the experiment, all substrings are biased at 3 A. Then, power is reduced in one of the substrings. The 100% mismatch corresponds to this substring being at zero power.

When the subMIC power limit is not reached, the system operates in the same manner as the system with full-power rated subMICs. When the power limit is hit, the system

characteristic changes. Figure 5.4 shows the PV curves under extreme mismatches. The 80% mismatch corresponds to 600 mA biasing and 90% mismatch corresponds to 300 mA bias current.

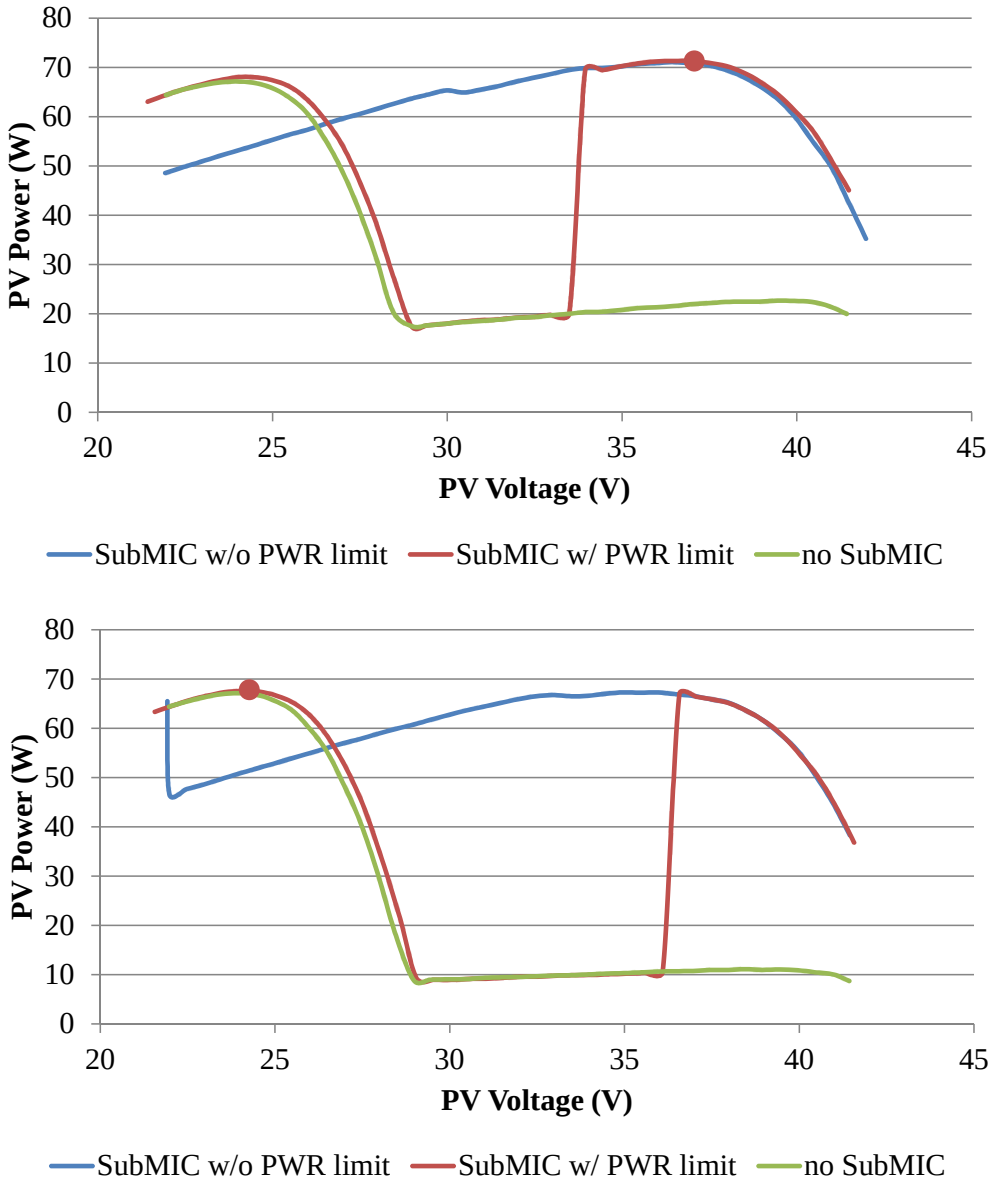


Figure 5.4: PV sweep of power limited subMICs under 80% mismatch (top) and 90% mismatch (bottom).

Starting from the highest PV voltage, it is observed that the power limited subMIC system behavior is similar to the full power rated subMIC system. As the PV voltage is lowered, the subMICs are demanded to process more current. Then, when the power limited subMIC cannot process the current demanded, the subMIC enters the *Limit* mode and turns off. From this point and down, the PV curve of the power limited subMIC system follows the PV curve of the conventional case, with the corresponding bypass diode conducting.

Two different characteristics are observed for power limited subMICs. First, the single maximum benefit of the subMIC system is lost. Second, the power limited subMIC system can actually have a higher peak power than the full power subMIC under extreme mismatches. This is seen in the 90% mismatch case. A better view comparing the peak powers is shown in Figure 5.5.

First, observing the ideal case in the power plot, a linear drop in power is observed. The efficiency of the subMIC systems start at the ideal point at 0% mismatch. However, the power drops at a slightly steeper slope than in the ideal case. This is due to the subMIC converter efficiency. Both subMIC cases follow the same power slope until the 90% mismatch point. At the 100% mismatch point, the power limited subMIC follows the power curve of the conventional system.

It is interesting to note that the full power rated subMIC system can perform worse than the conventional system at extreme mismatch. However, this is not a concern in practice. The mismatch distribution in realistic scenarios is heavily weighted at under 20% mismatch, and extreme mismatches are highly unlikely.

Indoor experimental results confirm that the DPP subMIC systems can significantly improve performance over conventional PV systems. This is possible even with only 90% efficient converters at a much lower power rating compared to the PV substring power rating. The full power rated subMICs are not the optimal design for DPP systems. Also, due to limited subMIC efficiency, simply turning off the subMICs in extreme mismatch cases improves the overall system performance.

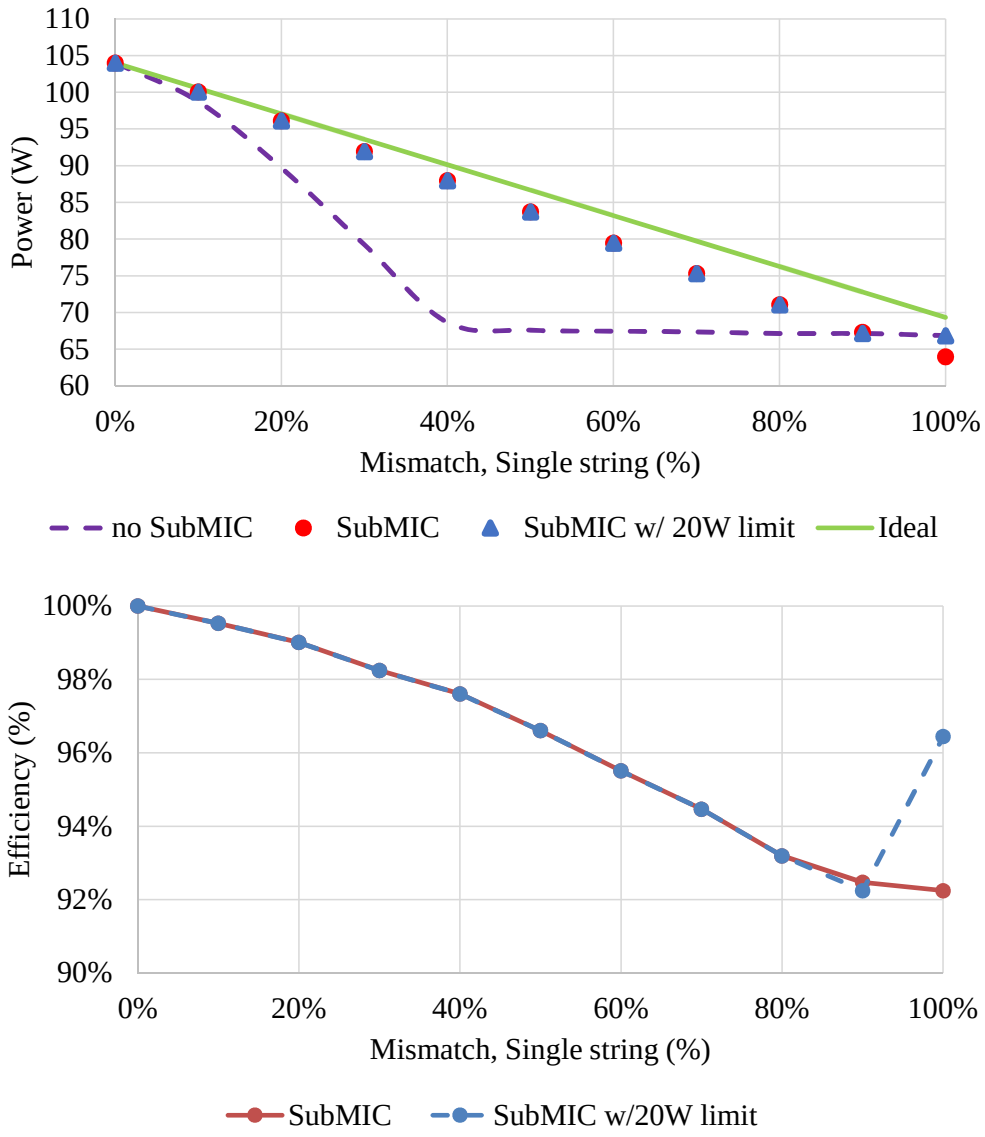


Figure 5.5: Power (top) and efficiency (bottom) versus a single substring mismatch plots.

5.2 Outdoor Experiments

Outdoor experiments are performed to evaluate performance under realistic insolation and shading conditions. The bench experiments performed in the previous section could be significantly different from experiments performed in the field. First, the series resistances in the PV are biased in the opposite direction under actual insolation. Also, the PV panels

tend to heat up under sunlight, while shaded portions remain at a lower temperature. This causes a lower V_{oc} for the higher power generating substrings.

The prototype board with three subMICs power limited to 20 W is installed into the PV junction box as shown in Figure 5.6. The four port voltages of the subMICs are probed

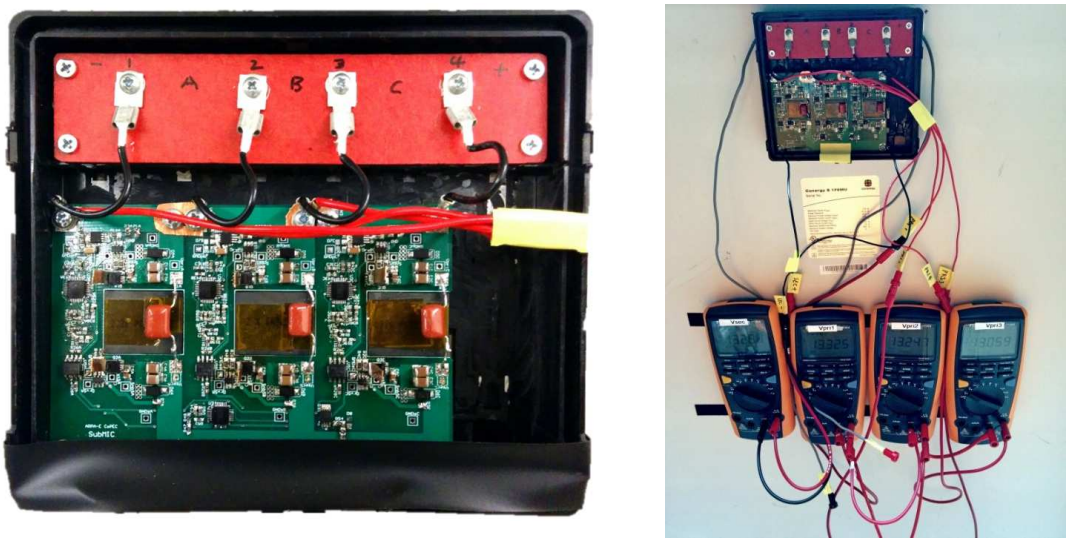


Figure 5.6: SubMIC prototype placed inside the junction box of a 175 W PV module.

behind the PV module to examine the operation of the subMICs. The PV module is taken outside with a DC load capable of performing a voltage sweep.

5.2.1 Substring Shading

The first outdoor experiment is done with a uniform shade over a single substring as shown in Figure 5.7. Tinted acrylic panels are used as shades.

This allows for a more controlled shading where all the PV cells in the substring see the same shading. It is expected that none of the PV cells will be in the second quadrant operation. The shading is done in three increments: clear (0%), low tint (5%), and high tint (29.5%). Experiment is performed on a clear day with 1000 W/m^2 sunlight with the PV

Figure 5.7: Shading pattern for the fully shaded substring.

module standing on concrete.

The maximum power results between the subMIC and the conventional case are compared in Table 5.3. For the clear-sky scenario where there should be no mismatch, it is observed that the subMIC case performs slightly better than the conventional case. This is not expected since the subMICs do consume some power even under no mismatch condition. Similar results were obtained in multiple trials. It is possible that inherent mismatches due to parameter tolerances are present in the PV module. This mismatch is mitigated by the subMICs, which is why the subMIC-enhanced module performs slightly better than the same module with conventional bypass diodes under no-mismatch condition.

	Clear	Low tint	High tint
w/o SubMIC	155.2 W	150.9 W	122.6 W
SubMIC	155.7 W	152.3 W	138.3 W
Improvement	0.3 %	1.0 %	12.8 %

Table 5.3: MPP power from the substring shading experiment.

In order to compare the results to the indoor experiment results, the 155.7 W result

is taken as the ideal case power reference. Then, the tint shade value is used to extrapolate the ideal power for the shaded cases. Figure 5.8 shows the power versus mismatch plot with the ideal case included.

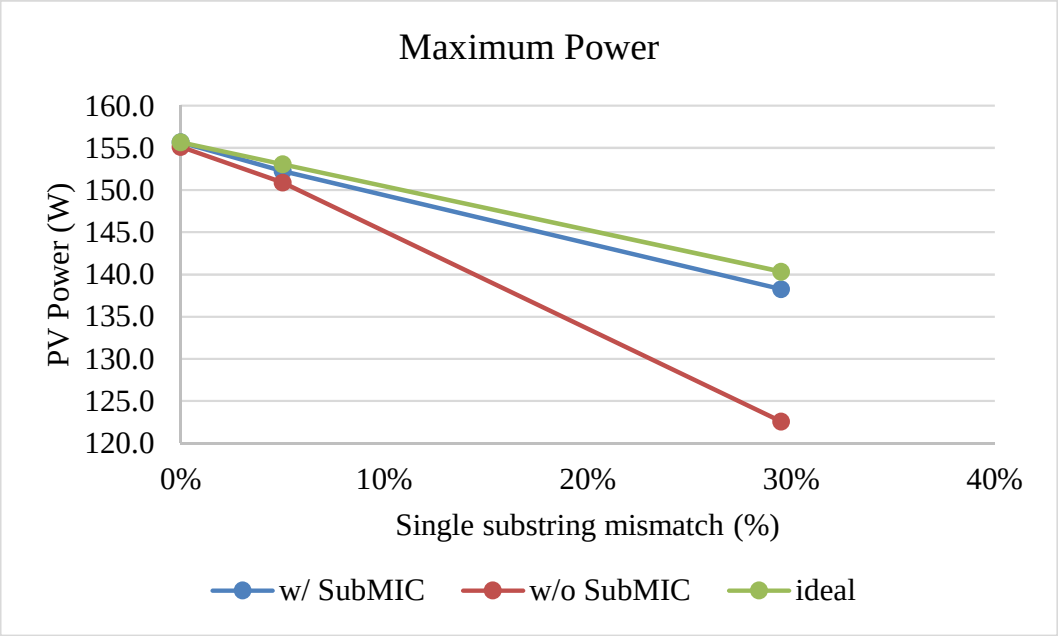


Figure 5.8: Power versus mismatch plot for the outdoor substring shading experiment.

Results show that the output power of the subMIC-enhanced PV module closely follows the ideal curve as in the indoor experiments. Using the ideal case power, efficiency of the tested cases can be evaluated. The no-shading case with subMICs is considered to be the 100% efficiency reference case. The results are shown in Table 5.4.

	Clear	Low tint	High tint
w/o SubMIC	99.7 %	98.6 %	87.3 %
SubMIC	100 %	99.5 %	98.5 %

Table 5.4: Efficiencies of the substring shading experiment.

The high tint results can be compared to the 30% mismatch results in the indoor experiments. Even though the indoor experiments were performed under 30% lower power,

the subMIC efficiency is very similar.

Next, the PV curves of the experiment are shown in Figure 5.9. As in the indoor experiments, the subMIC case shows very small variances in V_{MPP} for change in shading. On the other hand, the conventional case shows an increase in V_{MPP} as shading increases.

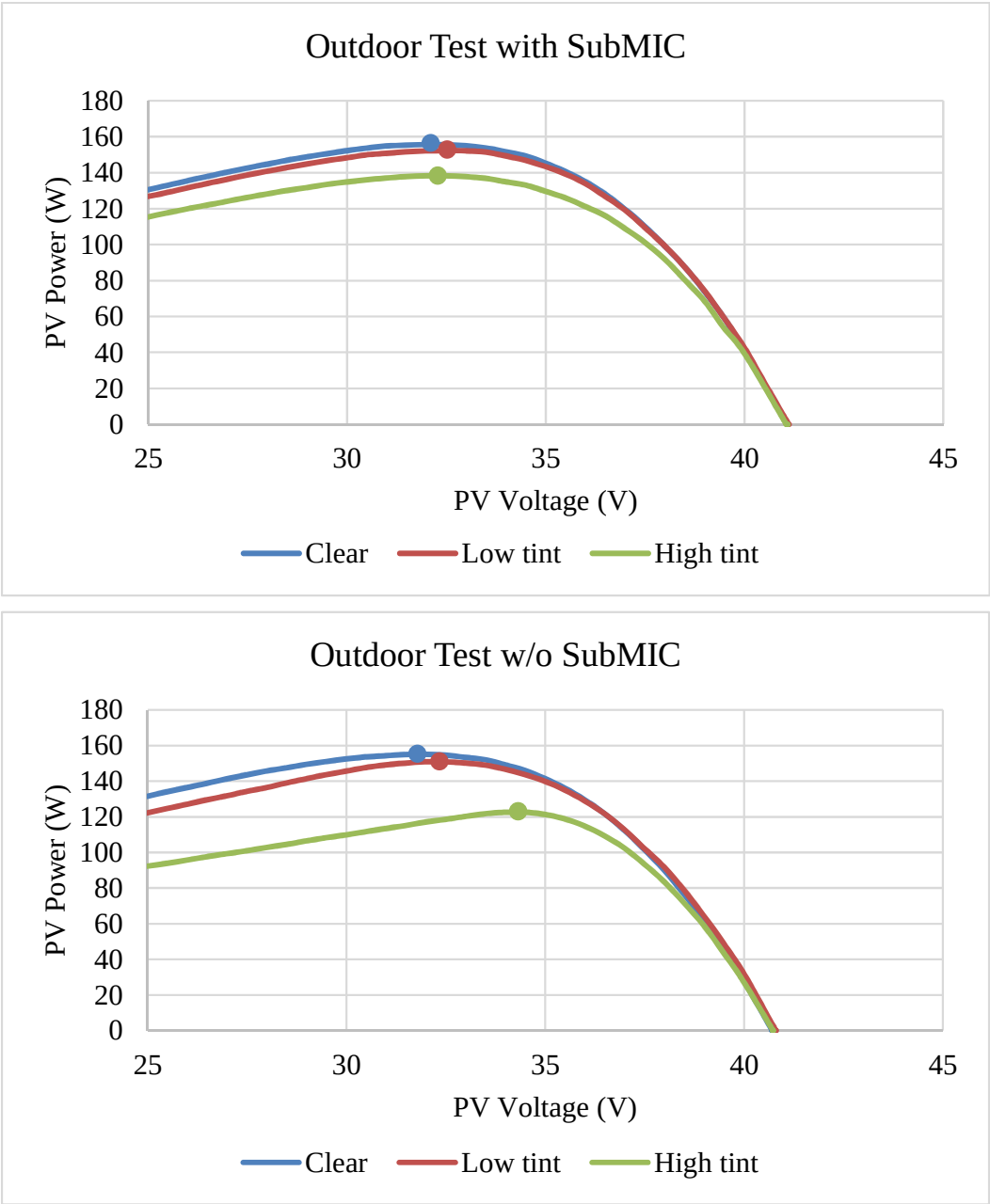


Figure 5.9: PV curve of the conventional (bottom) and subMIC (top) system with substring shading

The controlled substring level shading experiment shows that the results agree with the indoor bench experiments.

5.2.2 Partial Substring Shading

In this experiment, a more realistic shading pattern is used. However, the pattern is still generated in a controlled manner. Like the shading panels used in the experiments in Subsection 5.2.1, tinted acrylic panels are used to control the shading, but at a smaller size. The shading panels are designed to only cover four PV cells as shown in Figure 5.10. Now there is a mismatch created among the series PV cells within a substring. This would result in an increase in the corresponding V_{MPP}. The shading patterns considered are now at 30% and at 60% shade.

Figure 5.10: Shading pattern for the partial shaded substring.

First, the characteristics of a partially shaded substring is examined by measuring the IV curve of a single substring with shading. The experiment is performed under 500 W/m^2 sunlight. Results are shown in 5.11.

Unlike the PV or IV curve expected for insolation differences, the partial shading results show sharper transitions in the curves when shading increases. As a result, V_{MPP} moves more towards V_{oc}. It also shows relatively large deviance in V_{MPP}, which could

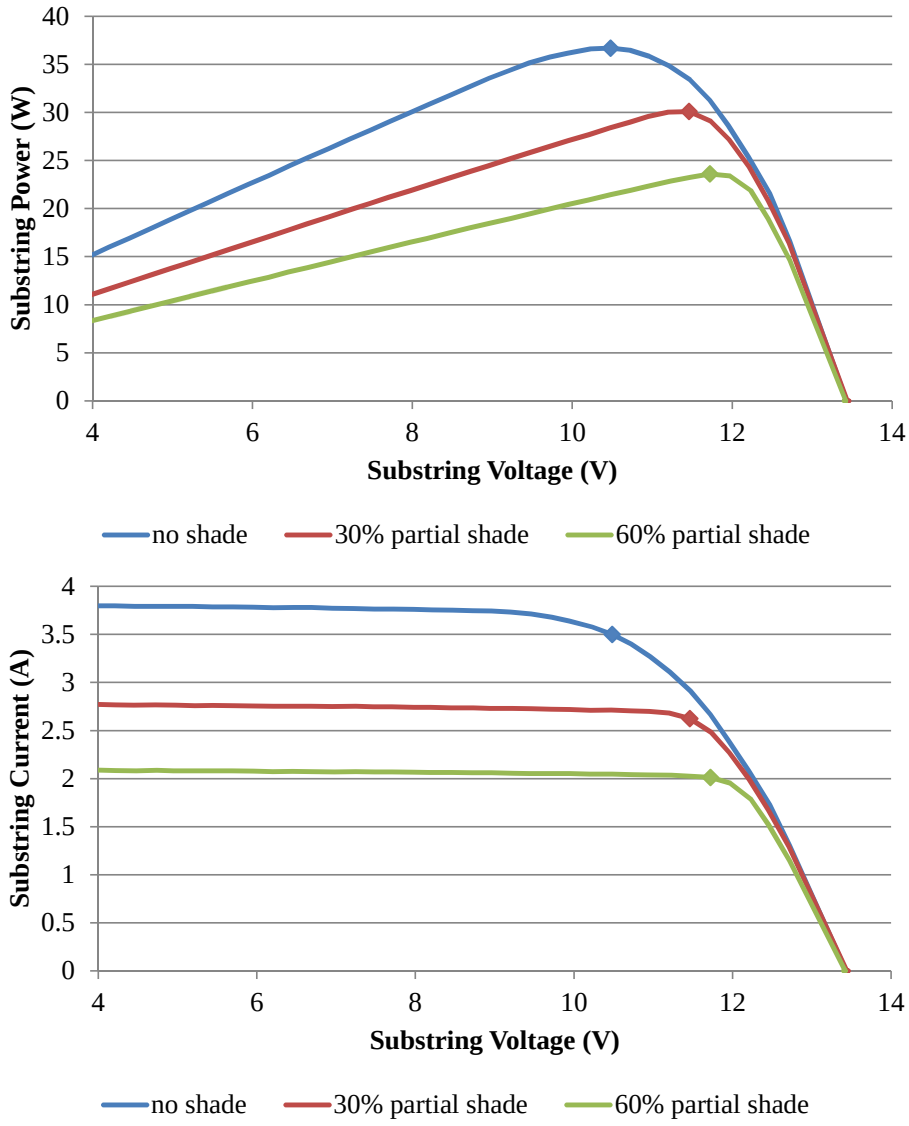


Figure 5.11: PV (top) and IV (bottom) curve of a substring with partial shading

affect the performance of voltage balancing controls. In voltage balancing control, it has been assumed that the substring V_{MPP} are all approximately the same. With 30% shading, almost a volt of increase in V_{MPP} is observed. In the perspective of power drop between the shading levels, the power drops by about 18% for every 30% step in shading.

Next, PV voltage sweeps are performed with the partial shading. The experiment is

performed under 700 W/m^2 sunlight. The results are shown in Figure 5.12.

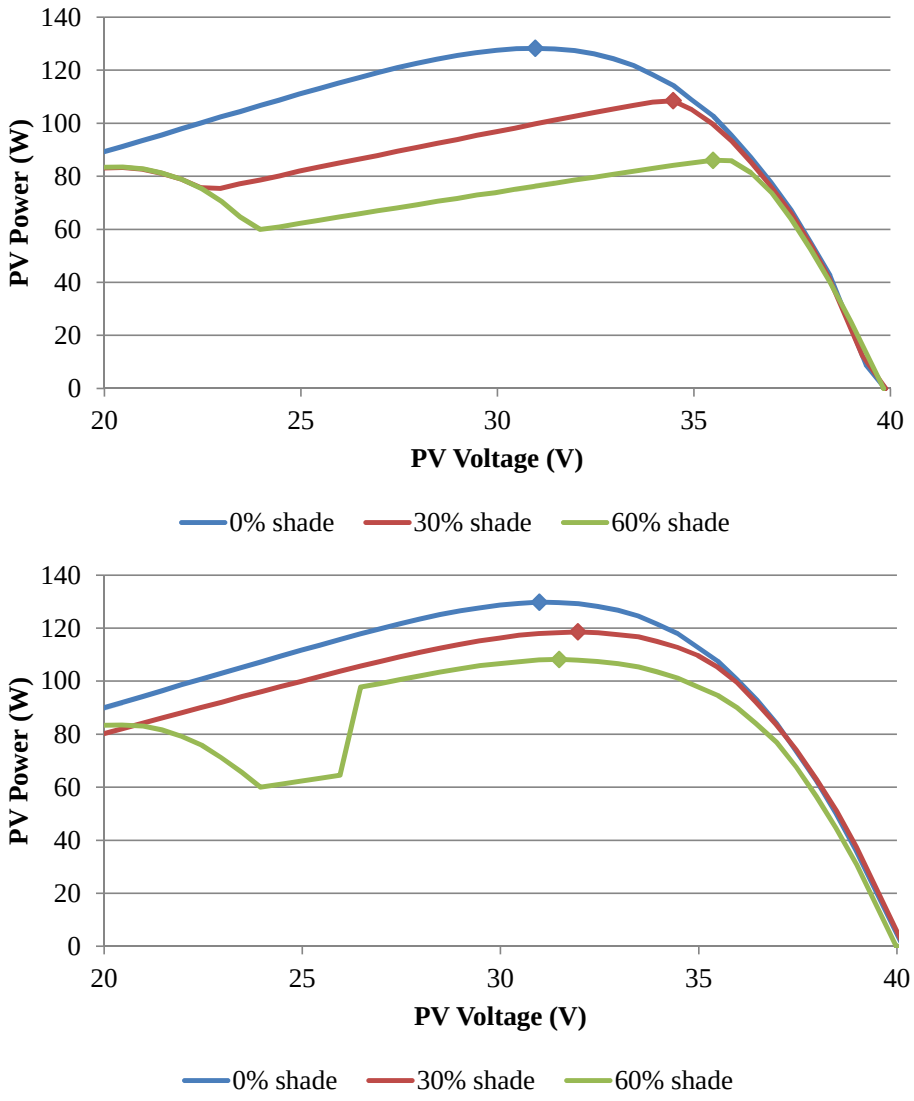


Figure 5.12: PV curve of partial shading on a substring for a conventional (top) and power limited subMIC (bottom) system.

Compared to the other experiments, the PV curves show different characteristics. First, the PV curve of the conventional case shows the steep curve transition observed in the single substring analysis. However, the V_{MPP} at 30% shading does not deviate much more than what is observed in the 30% substring level shading. The power limited subMIC results

show that V_{MPP} is maintained within a volt range. Also, a lower power drop is observed compared to the conventional case. The output power for each case at MPP is shown in Table 5.5. Again, the subMIC-enhanced module shows slightly better performance than

	0 % shade	30 % shade	60 % shade
w/o SubMIC	128.2 W	108.5 W	86.0 W
SubMIC	129.8 W	118.6 W	108.2 W
Improvement	1.2 %	9.3 %	25.8 %

Table 5.5: MPP power from the substring partial shading experiment.

the conventional system in the no-shading case. Compared to the 12.8% improvement the subMICs contributed in the 30% shading case in the previously considered substring-level shading, the subMICs now show a slightly less 9.3% performance improvement over the conventional system. The conventional system actually performs slightly better under partial substring shading compared to the uniform substring shading case, while the subMIC system performs slightly worse.

5.3 Analysis of the Performance Testing Results

The power limited subMICs are shown to improve performance of the PV system under mismatches when compared to the conventional setup with bypass diodes only. Also, the V_{MPP} is maintained close to the nominal value under mismatch conditions. Performance is verified under both indoor laboratory environment and outdoor test environment. Compared to full substring level shading, the performance of the subMIC system was slightly degraded under partial substring shading. However, the subMIC-enhanced PV module shows significant improvements over the conventional system in all experiments.

Chapter 6

Design Optimization of SubMICs for DPP PV Systems

Performance of the DPP PV system depends on the mismatch scenario and the design specifications of the subMICs. In [36], energy yield improvements up to 7-11% have been evaluated for different mismatch scenarios. The scenarios also include different sets of PV module rating, subMIC power rating and efficiency. Obviously, a more efficient and higher power rated subMIC would shows better performance for most scenarios. However the cost and size of the subMICs would increase as a trade-off.

It has been shown in Chapter 3 that the size of the subMICs can be sufficiently small to fit in a commercial PV junction box at 60 W rating. This is over 50 % of the substring power rating of most commercially available PV modules, and is more than sufficient the DPP system. However, cost has not been yet discussed for the subMIC boards designed. System performance improvement should be compared to the cost of the design.

In the following section, cost model for the prototype subMIC is evaluated. Also, reduced cost designs using a proposed new subMIC controller IC architecture is proposed. Cost evaluation is performed for the new subMIC design sets. The sets vary in cost, power rating, and efficiency. An evaluation method is also presented to compare the design using a cost/performance based figure of merit for different PV system mismatch scenarios. Finally, optimal subMIC designs for each scenario is selected and evaluated.

6.1 Cost Modeling SubMICs based on Power Rating

First, the cost of the prototype design is evaluated to identify the dominant costs in the subMIC prototype board. It is assumed that the subMICs will be produced in high volume count over 10000. The cost of subMICs can be divided in to the following costs:

- Semiconductors
- Magnetics
- PCB
- Passives

Semiconductor and passive component costs for power converters have been evaluated before in [37–39]. For our evaluation, component costs for semiconductor and passives are collected from internet suppliers [40, 41]. The costs found for the prototype are shown in Table 6.1. Here, the cost of resistors and capacitors are negligible compared to the semiconductor costs, hence neglected. Furthermore, the custom subMIC controller is estimated to be $.50 based on cost of other power converter ICs available at similar sizes.

Table 6.1: Estimated component costs

Type	**Cost ($)**
Power MOSFET	$ .10
Gate driver	$ .20
Zener diode	$ .10
LDO	$ .10
Digital isolator	$ .50

Magnetic core and PCB costs is modeled using the curve-fit based results from [37]. The models are shown in the following:

$$COST_{core} = (1 + a_{margin}) \cdot \sigma_{core} kg_{core} \tag{6.1}$$

$$COST_{PCB} = A_{adjust}(a_{area} + b_{area}A_{PCB}) \cdot (a_{ounce} + b_{ounce}H_{PCB}) \cdot (a_{layer} + b_{layer}N_{PCB} + c_{layer}N_{layers}^2) \quad (6.2)$$

The core cost increases as a linear function of material cost per kilogram (σ_{core}), core weight (kg_{core}) and cost margin (a_{margin}). The PCB cost is more complex. PCB cost is a function of PCB area (A_{PCB}), copper thickness (H_{PCB}), and PCB layers (N_{layers}). Cost increases linearly with PCB area and copper thickness, but not for PCB layers. The ax, bx, and cx coefficients are the corresponding curve-fit coefficients adjusted to fit the current market costs. Values are shown in the following Table 6.2 and 6.3.

Table 6.2: Magnetic core cost coefficients

Coefficient	**Value**
σ_{core} ($/$_{kg}$) (high performance ferrite)	6.6
a_{margin}(%)	200%

Table 6.3: PCB cost coefficients

	ax	***bx***	***cx***
$\boldsymbol{A_{PCB}}$	0.4884 ($^{1/3})	388.8 ($^{1/3}/m^2)	
$\boldsymbol{H_{PCB}}$	10.1868 ($^{1/3})	2.8994 ($^{1/3}/Oz)	
$\boldsymbol{N_{layers}}$	0.03529 ($^{1/3})	-3.333x10^{-3} ($^{1/3})	2.195 x10^{-3} ($^{1/3})

* A_{adjust}=0.5

The cost of the prototype subMIC is estimated based on this model. For the initial analysis, planar magnetic PCB is assumed to be a separate PCB from the main PCB: which consists of 8 layers with $3oz$ copper. The cost budget is shown in Table 6.4.

Comparing the cost budget, PCB costs are the most significant. The next most significant are the special semiconductors: isolators and drivers. Analysis shows the cost per converter power rating (3x 60 W) to be about \$.06/W. Compared to a 300 W PV module, this would be about \$.035/W. The cost budget does not include assembly costs such as integrating the magnetic components to the board. These costs could increase the total cost. In

Table 6.4: Prototype subMIC cost estimate

	Type	**$/count**	**Count**	**Total ($)**
1	Main PCB	1	1	1
2	MOSFET	0.1	6	0.6
3	Driver	0.2	6	1.2
4	Magnetic Core	0.1	3	0.3
5	Planar PCB	1	3	3
6	Zener	0.08	6	0.48
7	LDO	0.1	4	0.4
8	SubmicIC	0.5	4	2
9	Digital isolator	0.5	3	1.5
			Total sum ($)	**10.48**

the next section, a more optimized design which reduces cost of components and assembly cost is presented.

6.2 Reduced Cost SubMIC Designs

In the cost budget of the prototype design, significant fraction of the cost were from special semiconductors. If these components could also be integrated into the subMIC IC, cost can be significantly reduced. The prototype subMIC IC outputs were designed to adequately drive small MOSFETs at reasonable speeds. Gate drivers for both the primary and secondary side MOSFETs can be integrated with minor adjustments. Also, the secondary side voltage can be sensed through the primary side winding as done in commercially available ICs [42,43] during the secondary side conducting phase. Hence, there would be no need for the isolators. Furthermore, the LDO can be also integrated into the subMIC IC.

A conceptual improved subMIC IC design (rev.3) and the peripheral circuits are shown in Figure 6.1. The new design eliminates all extra ICs with the cost of extra gate driving circuitry for the secondary side.

Next, planar winding designs can be integrated into the main PCB. This will reduce the manufacturing cost, but it would significantly increase the overall PCB cost for the

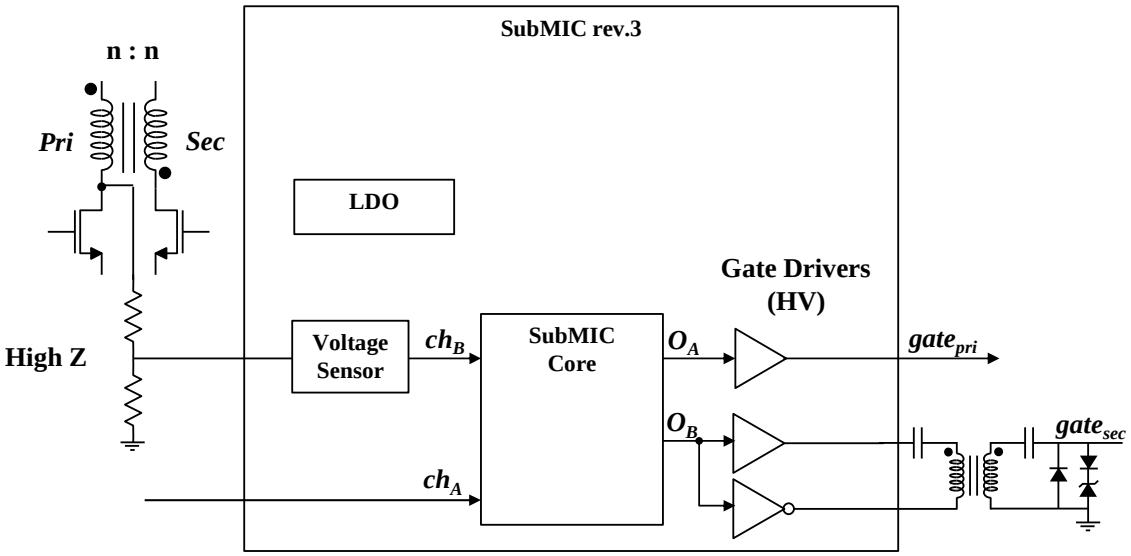


Figure 6.1: Block diagram of improved subMIC IC design with the rev. 2 subMIC core reused.

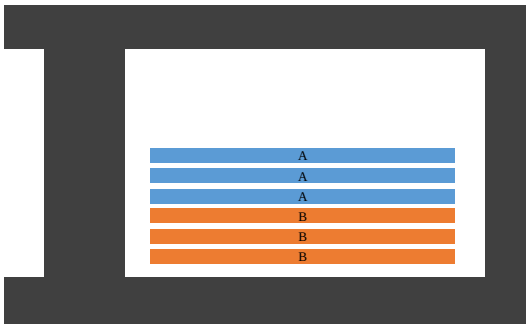
prototype design. Cost of the PCB can be reduced by redesigning the planar windings. By using less copper and winding layers, cost can be reduced significantly. The trade-off of the designs would be efficiency.

The new reduced cost subMICs are designed using the improved subMIC IC and reduced cost planar winding designs. It assumes that the main PCB size and magnetic core selection does not change with design. However, the planar winding design is varied in both copper ounce and winding configuration. Copper ounce is varied from 1 to 3 oz, and the winding configurations are shown in Figure 6.2. Winding design considers both 3 and 4 turns for the designs. Planar design specifications, such as the inductance, airgap, and switching frequencies, are shown in Table 6.5. Adjustments to the design for n=3 are done assuming A_e, I_{pk}, and B_{pk} are fixed so that the system gains are identical.

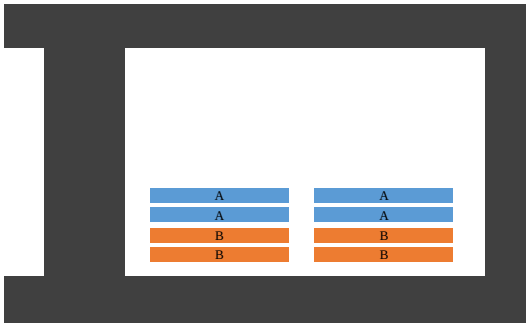
Total of 12 designs (combination of 1-3 oz copper and 4 winding configurations) are designed. The loss estimation method used for the prototype subMIC is used for the new

Table 6.5: Magnetic specifications for different turns

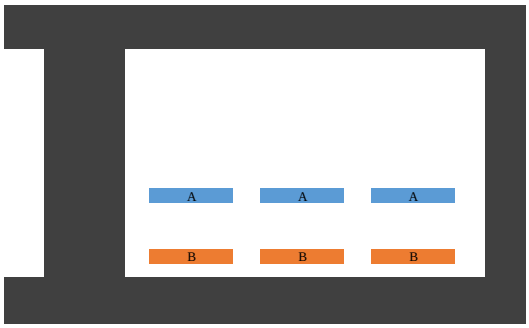
Winding turns (n)	**Inductance (uH)**	**Airgap (mil)**	***fs* (kHz)**
4	7.3	3	100
3	5.475	2.25	133



< n=3, 6 layers >



< n=4, 4 layers >



< n=3, 2 layers >

Figure 6.2: Planar magnetic designs with different PCB layers and turns.

designs. Efficiency curves are shown in Figure 6.3, 6.4, and 6.5. From the results, the design efficiency and power rating(limit) are determined. The efficiency of the converter is assumed to be the peak efficiency. The power rating is assumed to be the power at the peak efficiency point. This assumption can be considered valid since the efficiency curve of the prototype subMICs maintains peak efficiency lower loads.

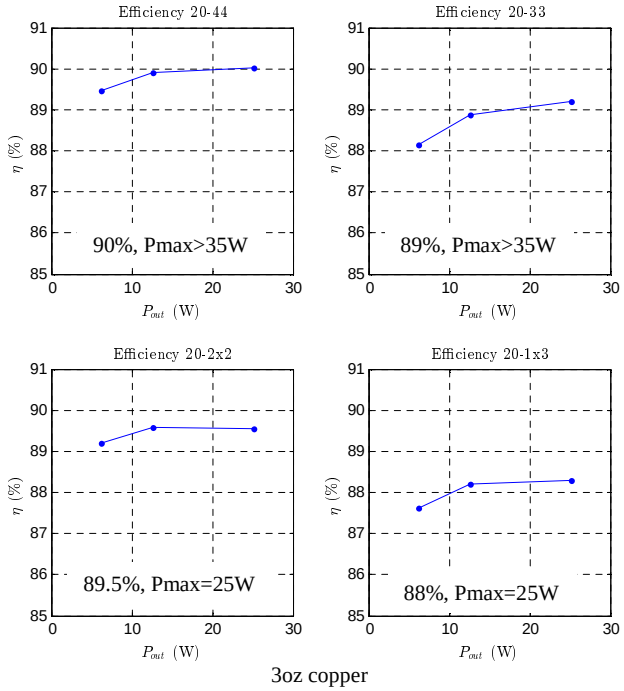


Figure 6.3: Evaluated efficiencies for 3 oz copper planar magnetics design.

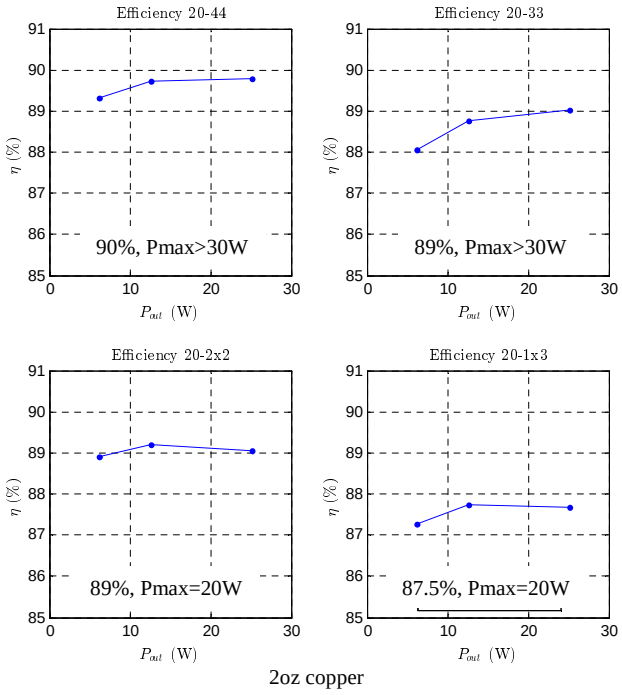


Figure 6.4: Evaluated efficiencies for 2 oz copper planar magnetics design.

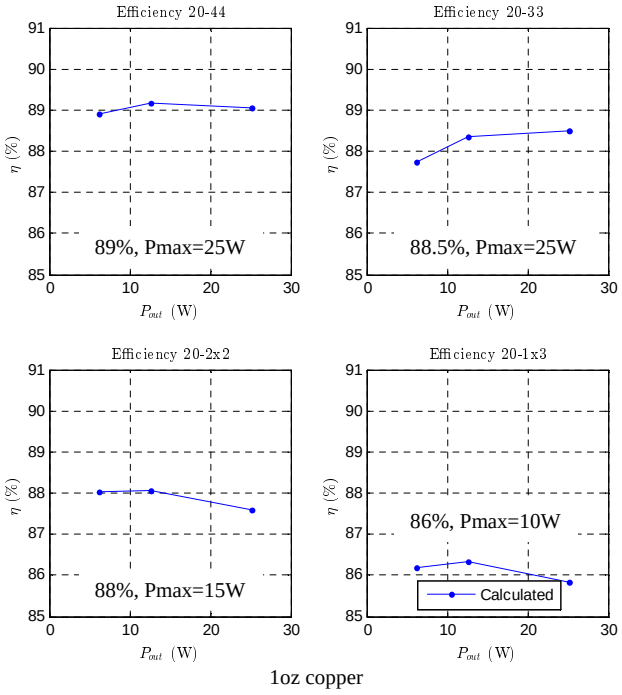


Figure 6.5: Evaluated efficiencies for 1 oz copper planar magnetics design.

The results can be organized to show the subMIC cost, efficiency, and power rating(limit) of the associated design. Results are shown in Table 6.6:

$$[Cost_{subMIC}, \eta_{conv}, P_{limit}] = f_{eval}([design\_set]) \tag{6.3}$$

Table 6.6: Efficiencies, power limits, and estimated costs of designs

Set #	Winding	Pmax (W)	Efficiency (%)	Copper (Oz)	Layers (n)	Cost ($)**	300W panel ($/W)***	200W panel ($/W)***
12 (*11)	20-44	35	90.0%	3	8	11.88	0.04	0.06
11 (*10)	20-33	35	89.0%	3	6	9.48	0.03	0.05
10 (*9)	20-44	30	90.0%	2	8	10.88	0.04	0.05
9 (*N/A)	20-33	30	89.0%	2	6	8.78	0.03	0.04
8	20-2x2	25	89.5%	3	4	7.78	0.03	0.04
7	20-1x3	25	88.0%	3	2	6.88	0.02	0.03
6	20-44	25	89.0%	1	8	9.88	0.03	0.05
5	20-33	25	88.5%	1	6	8.18	0.03	0.04
4	20-2x2	20	89.0%	2	4	7.38	0.02	0.04
3	20-1x3	20	87.5%	2	2	6.58	0.02	0.03
2	20-2x2	15	88.0%	1	4	6.98	0.02	0.03
1	20-1x3	10	86.0%	1	2	6.38	0.02	0.03

* Set # for scenario 4 in later sections
** Cost is for 3 converters
*** SubMIC cost per PV rating

With reference to the cost ($10.48) of the prototype subMIC, the #12 design ($11.88) is identical in specifications. The cost increase due to the unified PCB design in #12 is higher, but not much different. This is due to the reduce component costs of the new designs.

For each identical power rated design, cost of the converters decrease as the efficiency also decreases. This is due to the trade-off of reduced cost magnetic design.

In the following sections, the subMIC design sets are used to evaluate PV system performance improvements and analyze how each specification affects overall performance.

6.3 Evaluating System Performance of SubMIC Designs

SubMIC designs can optimized to be of different costs, efficiencies, and power ratings. Given the designs, it is not clear which design gives the best performance for the cost. Furthermore, it is also not clear whether or not a single design is the best choice for all possible PV system installments. In this section, the subMIC design sets from Section 6.2 are evaluated using a PV system simulation for differential power processing (DPP) [44, 45] under different PV system scenarios.

The diagram in Figure 6.6 shows an overview of how the evaluation is performed. First, the design set specifications are reorganized. The subMIC costs is a function of converter efficiency (η_{subMIC}) and power rating (P_{limit}).

$$Cost_{subMIC} = f_{cost}(\eta_{subMIC}, P_{limit}) \tag{6.4}$$

Then, the same sets of efficiency and power rating are evaluated in the PV simulator. Obtained are the performance improvement ($\Delta E/E_{conv}$) achieved by each design set for a PV system scenario.

$$\Delta E/E_{conv} = f_{performance}(Scenario, \eta_{subMIC}, P_{limit}) \tag{6.5}$$

Performance improvement ($\Delta E/E_{conv}$) is defined as the following relationship of energy production from the DPP subMIC system (E_{subMIC}) and the conventional system (E_{conv}) using backplane diodes.

$$\Delta E/E_{conv} = 100 \cdot \frac{E_{subMIC} - E_{conv}}{E_{conv}} \tag{6.6}$$

Finally, subMIC cost to performance improvement relationship is obtained by combining the results.

The cost/performance plot in Figure 6.6 shows how the designs would distribute relative to PV module cost ($Cost_{PV}$) slope and the loss percentage of the conventional system

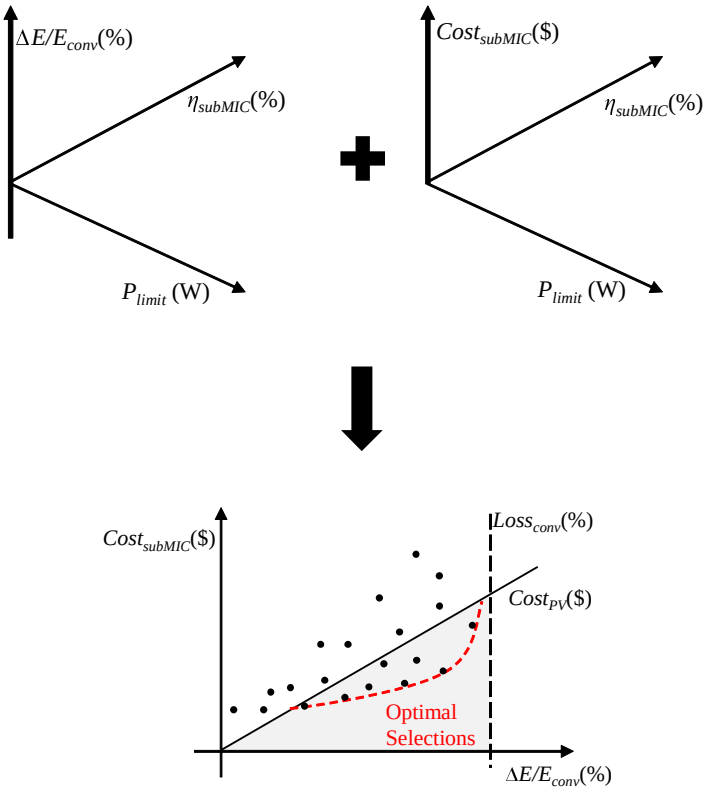


Figure 6.6: Optimal design selection scenario.

($Loss_{conv}$). Improvement cannot exceed the system loss from the conventional system, hence the designs are shown to the left of the loss line. Designs below the PV module cost line are which the cost of the subMICs are justified for the performance improvement. A measure is defined to quantify the cost justification: SubMIC Figure Of Merit (SFOM). The following equation defines the SFOM, where a value over 1 corresponds to justified cost.

$$SFOM = \frac{\Delta E/E_{conv}}{Cost_{subMIC}/Cost_{PV}} \tag{6.7}$$

The E/E_{conv} term is the performance improvement and $Cost_{subMIC}/Cost_{PV}$ is the cost overhead of the subMICs.

It must be noted that the definition of SFOM only takes in to account the costs of PV modules and subMICs for the cost overhead ratio. It does not take into account other balance of system costs. The cost justification would be different if these costs are considered. For

example, module level power electronics (MLPE) would improve energy extraction without the need of extra room for equipment. On the other hand, installing more PV panels would require more room and wiring, hence cost. Given that the popular DC optimizers currently out in the market is about $40-$80 per PV module (with cost range of $100-$300), the defined SFOM would come out to be far below the unit SFOM value of 1, suggesting the cost of the device is not justified. Hence, this measure is not a method to measure absolute feasibility of the devices, but only as a relative measure to evaluate performance versus cost of different subMIC designs. The SFOM presented is an example of a figure of merit for optimization purpose. It should be extended to include other balance of system costs in the future.

6.4 System Performance Comparison Results

In this section, the performance of the designs from the previous sections are evaluated under various ageing, mismatch, and PV module configurations. The scenarios are based on the ageing and shading data of residential and commercial systems used in [46]. The ageing scenarios have a uniform, but weak power mismatch distributed among the PV cells. On the other hand, shading scenarios have a more stronger and spatially localized power mismatch. Two types of evaluations are performed: ageing and shading scenarios. For each scenario, different PV systems with varying module power rating and setup are used. Figure 6.7 shows the block diagram of the evaluation and optimization process.

The scenarios evaluated can be summarized as the following Table 6.7. The scenarios are configured to evaluate how performance varies as mismatch levels increase (scenario 1 and 2 to 3 and 4), substring to subMIC power rating ratio changes(scenario 1 to 2 and 3 to 4), and configurations change.

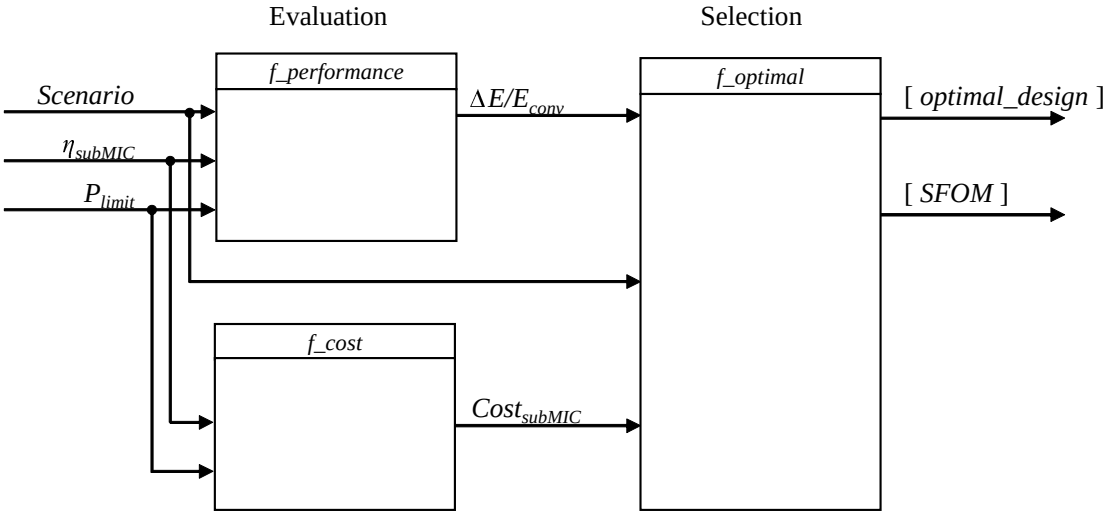


Figure 6.7: Block diagram of optimal design selection.

Table 6.7: Summary of PV system performance evaluation scenarios

Scenario#	Parallel strings	Modules per string	Module rating (W)	Mismatch scenario	Comment
1	2	7	185	Ageing	Reference (ageing)
2	2	7	318	Ageing	Increased rating (ageing)
3	2	7	208	Shading 1	Reference (shading)
4	2	7	297	Shading 1	Increased rating (shading)
5	1	16	189	Shading 2	Different system setup

6.4.1 Scenario 1: Ageing, 185W

This is a residential ageing scenario with 2 parallel strings of 7 series modules. The rating of the system is $V_{max} = 307$ V, $I_{max} = 10.6$ A, $P_{max} = 2.6$ kW. The PV module power level is considered as low compared to the 317 W panel in scenario 2. Hence, the power ratings of the subMICs would be at a higher percentage of the PV substring power rating than the other scenario. Specifications are shown in Table 6.8.

In this scenario, performance is evaluated at the 20 year point. The I_{mpp} and I_{sc} of the sub-strings are statistically varied so that the mean degradation is 0.8% per year based on the analysis done in [47]. The standard deviation is set to be 1% at year 1 and 10% at year

25. Average of 50 Monte-Carlo runs are shown as results.

Table 6.8: PV module specifications for scenario 1

EcoSolar	$92.8 @ $0.50/W		$185.6 @ $1.00/W		
Voc	44.9 V	Isc	5.3 A	Pmax	185 W
Vmpp	37.5 V	Impp	4.95 A	[Substring,Ncells]	[3,24]

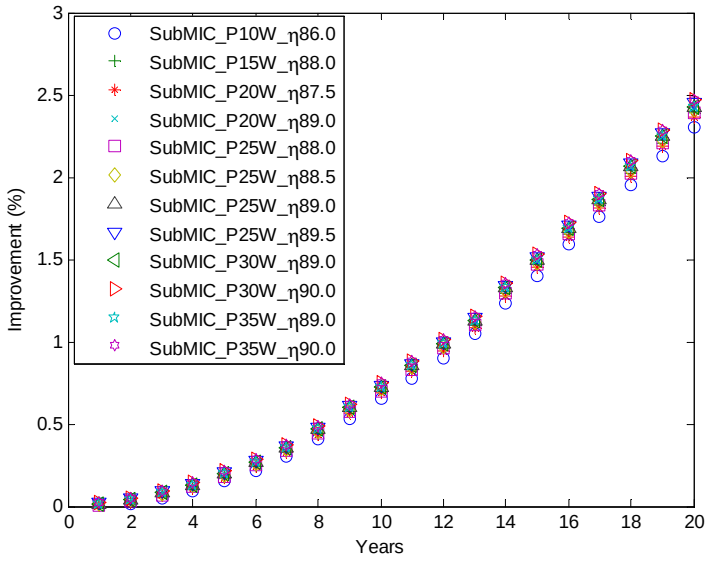


Figure 6.8: System efficiency improvement from subMICs at a given year for scenario 1.

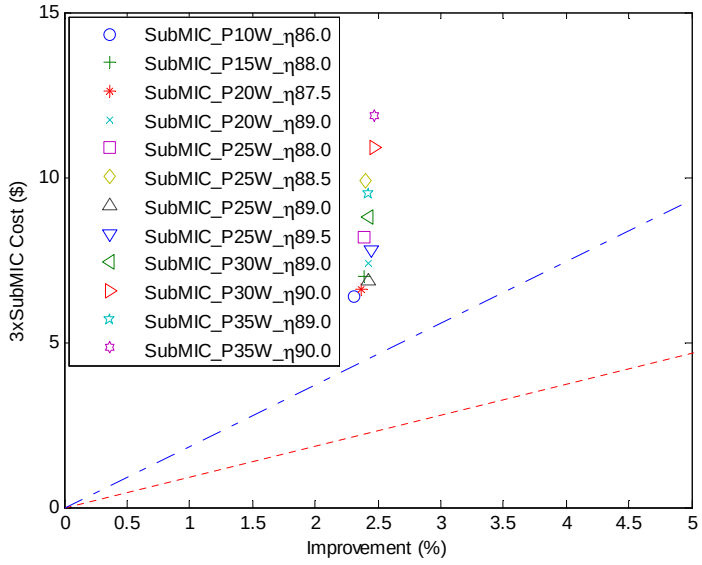


Figure 6.9: SubMIC cost versus improvement plotted over PV module cost justification line at :$1/W(dot dash) and $0.5/W(dot) for scenario 1.

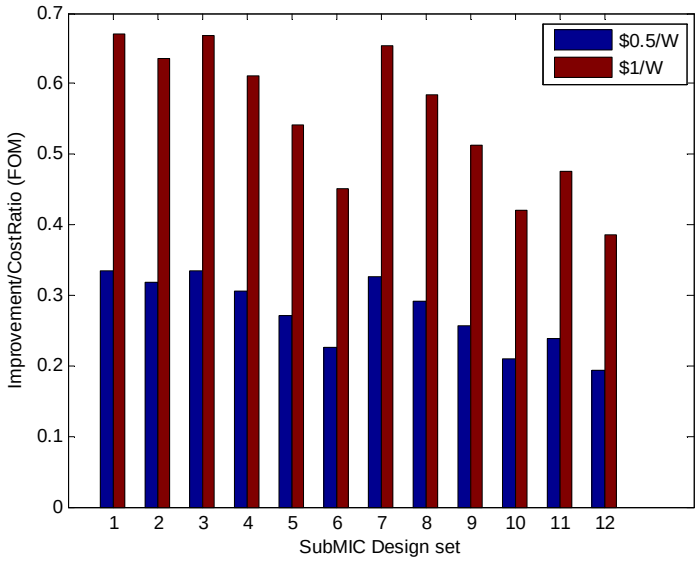


Figure 6.10: Figure of merit comparison of designs at PV module cost of $0.5/W and $1/W, where the first design set corresponds to the lowest power rated converter for scenario 1.

6.4.2 Scenario 2: Ageing, 318W

This is a residential ageing scenario with 2 parallel strings of 7 series modules. The rating of the system is $V_{max} = 321.3$ V, $I_{max} = 18.3$ A, $P_{max} = 4.45$ kW. This scenario uses PV modules with higher current ratings compared to scenario 1. Specifications are shown in Table 6.9.

In this scenario, performance is evaluated at the 20 year point. The I_{mpp} and I_{sc} of the sub-strings are statistically varied so that the mean degradation is 0.8% per year based on the analysis done in [47]. The standard deviation is set to be 1% at year 1 and 10% at year 25. Average of 50 Monte-Carlo runs are shown as results.

Table 6.9: PV module specifications for scenario 2

SolarWorld SW315	$158.8 @ $0.50/W		$317.6 @ $1.00/W		
Voc	45.9 V	Isc	9.16 A	Pmax	317.6 W
Vmpp	36.8 V	Impp	8.63 A	[Substring,Ncells]	[3,24]

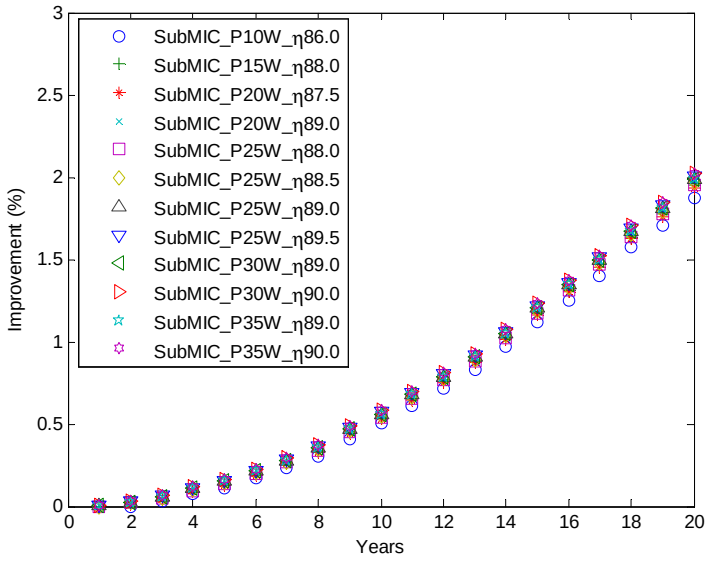


Figure 6.11: System efficiency improvement from subMICs at a given year for scenario 2.

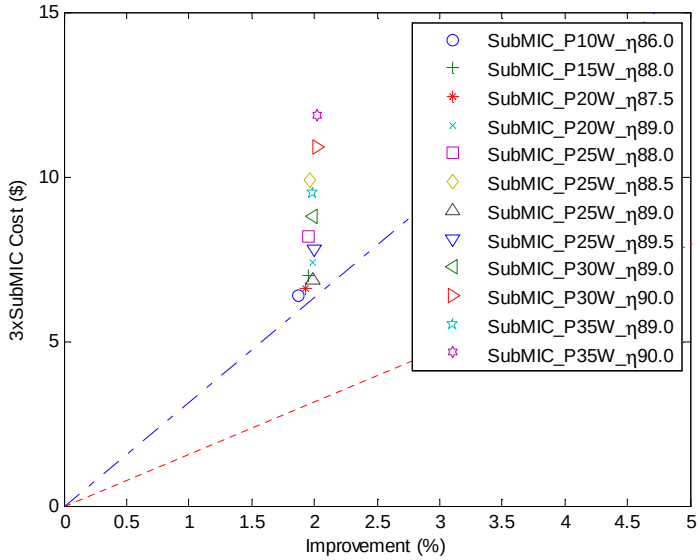


Figure 6.12: SubMIC cost versus improvement plotted over PV module cost justification line at :$1/W(dot dash) and $0.5/W(dot) for scenario 2.

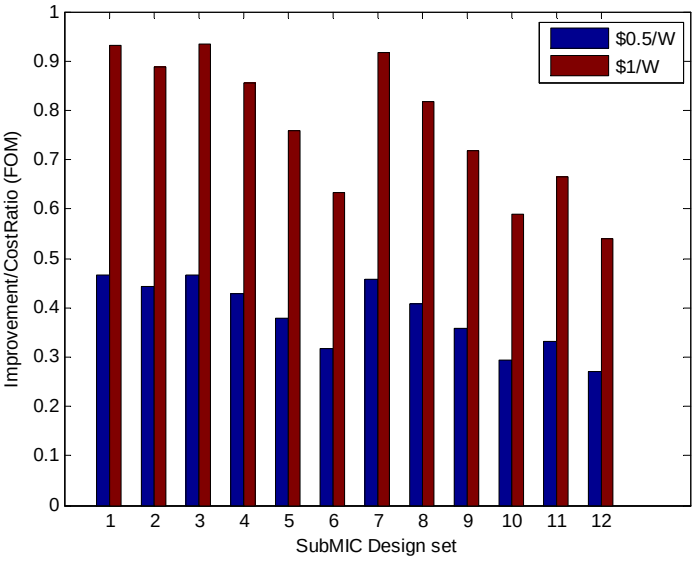


Figure 6.13: Figure of merit comparison of designs at PV module cost of $0.5/W and $1/W, where the first design set corresponds to the lowest power rated converter for scenario 2.

6.4.3 Scenario 3: Shading, 208W

This is a residential shading scenario with 2 parallel strings of 7 series modules. The shading pattern consists of shadow from a nearby tree sweeping over the PV installment [46]. The shadow covers direct sunlight, but still allow some indirect sunlight. The spatial resolution of the shadow is quite large enough to cover the whole system. This scenario is considered a scenario with weak mismatch due to shading compared to scenario 5.

Evaluation is done for a year of energy capture with I_{mpp} and I_{sc} of the sub-strings varied depending on the shading data. The rating of the system is $V_{max} = 252.7$ V, $I_{max} = 7.3$ A, $P_{max} = 2.91$ kW. Specifications are shown in Table 6.10

Table 6.10: PV module specifications for scenario 3

Sharp ND208	$104 @ $0.50/W		$208 @ $1.00/W		
Voc	36.1 V	Isc	8.1 A	Pmax	208 W
Vmpp	28.5 V	Impp	7.3 A	[Substring,Ncells]	[3,20]

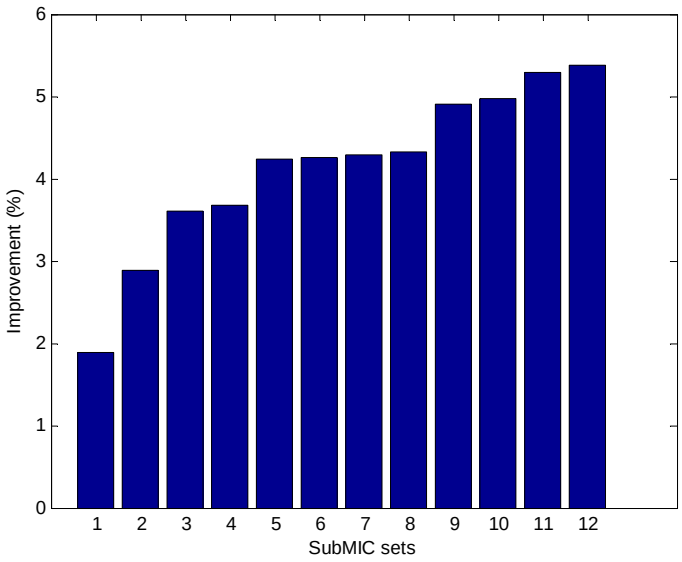


Figure 6.14: System efficiency improvement from subMICs, where the first design set corresponds to the lowest power rated converter for scenario 3.

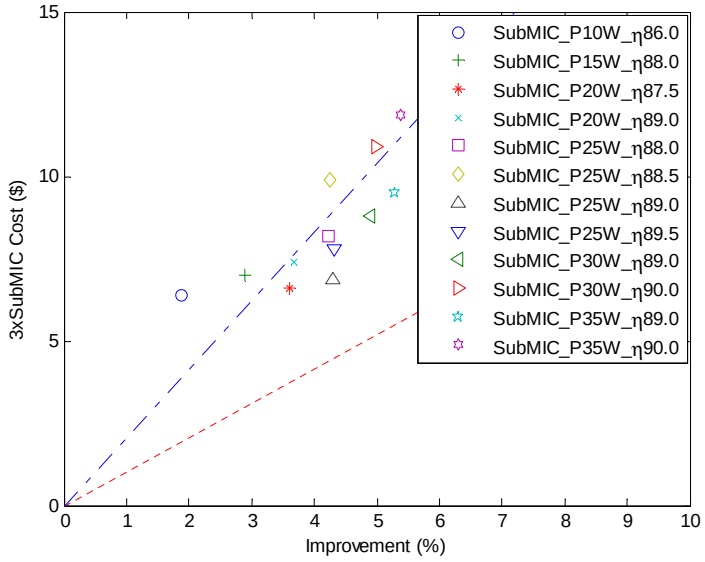


Figure 6.15: SubMIC cost versus improvement plotted over PV module cost justification line at :$1/W(dot dash) and $ 0.5/W (dot) for scenario 3.

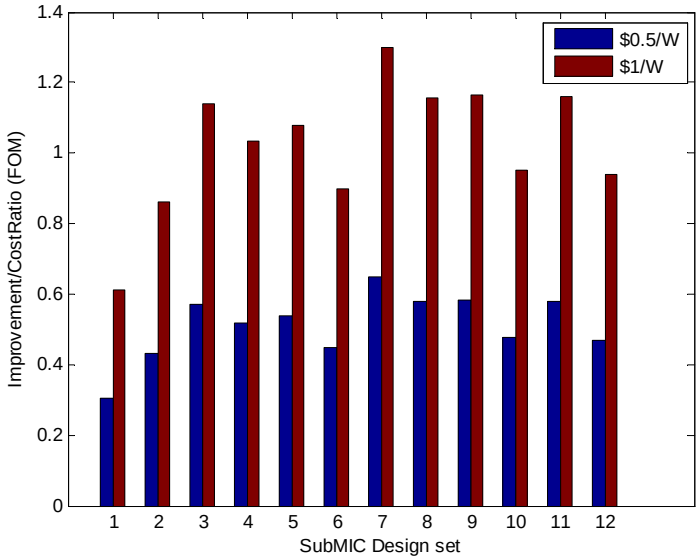


Figure 6.16: Figure of merit comparison of designs at PV module cost of \$0.5/W and \$1/W, where the first design set corresponds to the lowest power rated converter for scenario 3.

6.4.4 Scenario 4: Shading, 297W

This is a residential shading scenario with 2 parallel strings of 7 series modules. The shading pattern is identical to scenario 3. This scenario differs in power rating of the PV modules: 297 W. Evaluation is done for a year of energy capture with I_{mpp} and I_{sc} of the sub-strings varied depending on the shading data.

The rating of the system is V_{max} = 276.5 V, I_{max} = 10 A, P_{max} = 4.16 kW. This scenario has increase PV module power rating compared to the previous shading scenario. For this scenario, note that the 90% efficient 30 W converter is neglected in the evaluation due to convergence issues. Therefore design set [#10, #11, #12] are now [#9, #10, #11] for this scenario only. Specifications are shown in Table 6.11

Table 6.11: PV module specifications for scenario 4

LG 300	$148 @ $0.50/W		$296 @ $1.00/W		
Voc	39.5 V	Isc	10 A	Pmax	297 W
Vmpp	32.0 V	Impp	9.3 A	[Substring,Ncells]	[3,20]

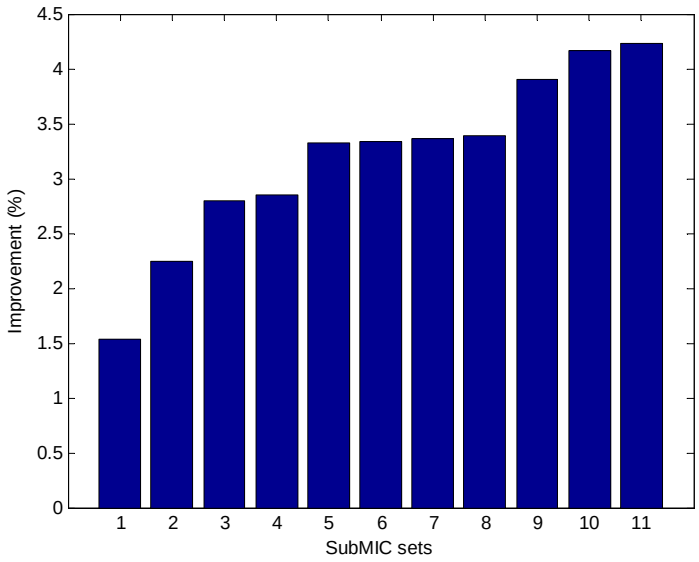


Figure 6.17: System efficiency improvement from subMICs, where the first design set corresponds to the lowest power rated converter for scenario 4.

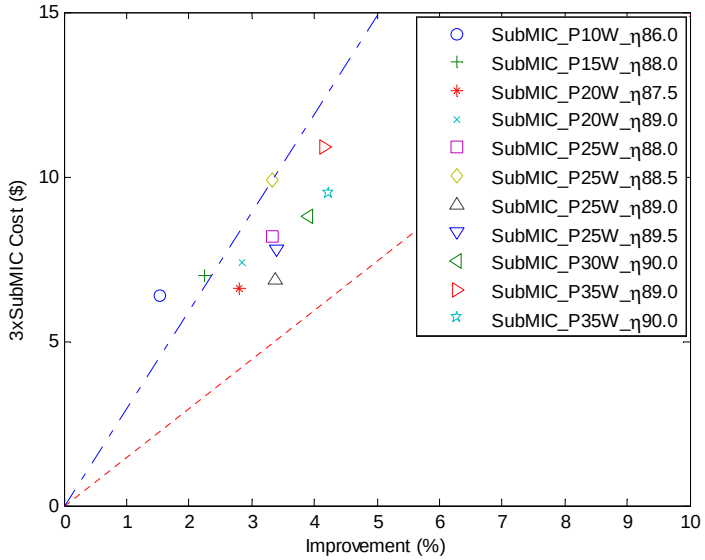


Figure 6.18: SubMIC cost versus improvement plotted over PV module cost justification line at :$1/W(dot dash) and $0.5/W(dot) for scenario 4.

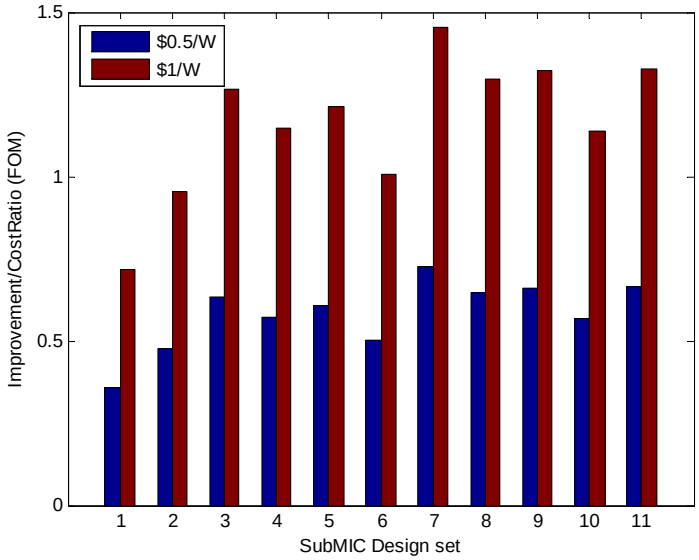


Figure 6.19: Figure of merit comparison of designs at PV module cost of $0.5/W and $1/W, where the first design set corresponds to the lowest power rated converter for scenario 4.

6.4.5 Scenario 5: Shading, 189W

This is a commercial shading scenario with a single string of 16 series modules is shaded by a adjacent lighting pole [46]. Compared to the residential shading scenarios 3 and 4, the shading pattern in this scenario is much more spatially sharp. The pole shade can be narrow as a PV cell. This scenario is considered a strong shading mismatch scenario.

The evaluation is done for a full day of energy capture with I_{mpp} and I_{sc} of the sub-strings varied depending on the shading data. The rating of the system is $V_{max} = 521.6$ V, $I_{max} = 8$ A, $P_{max} = 3$ kW. This scenario has increase PV module power rating compared to the previous shading scenario. Specifications are shown in Table 6.12

Table 6.12: PV module specifications for scenario 5

Unknown module	$94.6 @ $0.50/W		$189.2@ $1.00/W		
Voc	32.6 V	Isc	8 A	Pmax	189.2 W
Vmpp	26.4 V	Impp	7.2 A	[Substring,Ncells]	[3,36]

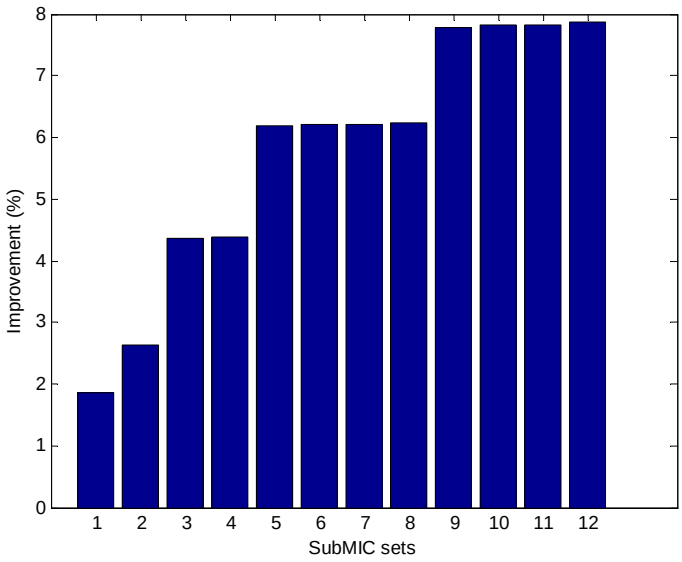


Figure 6.20: System efficiency improvement from subMICs, where the first design set corresponds to the lowest power rated converter for scenario 5.

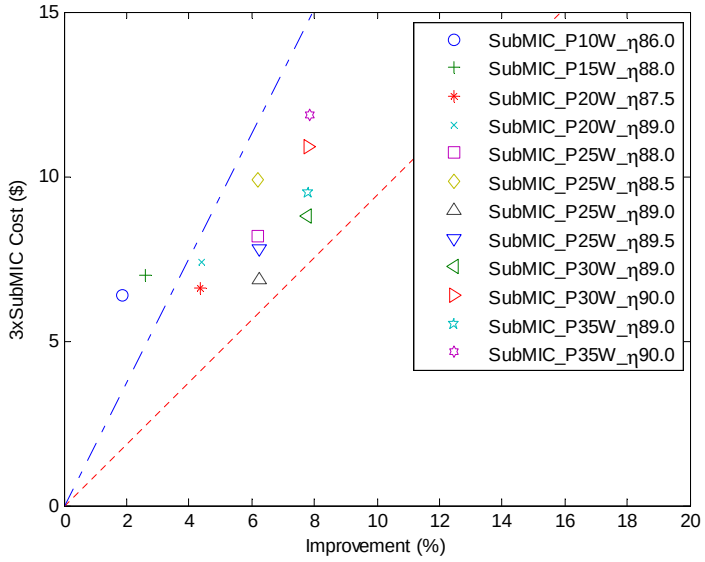


Figure 6.21: SubMIC cost versus improvement plotted over PV module cost justification line at :$1/W(dot dash) and $ 0.5/W(dot) for scenario 5.

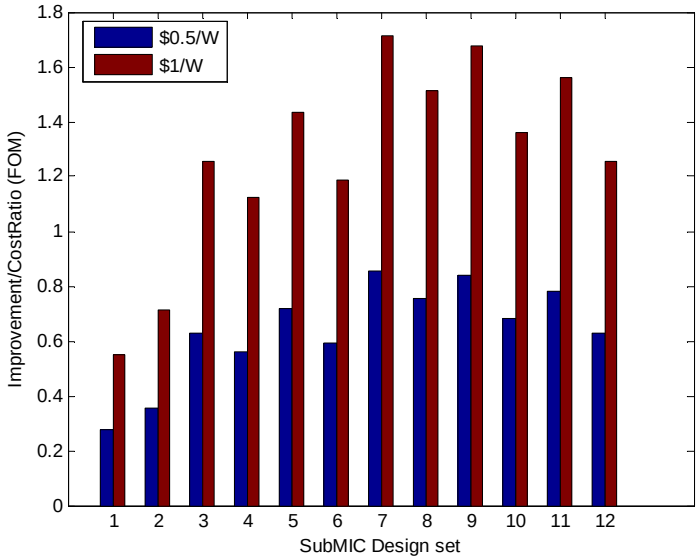


Figure 6.22: Figure of merit comparison of designs at PV module cost of \$0.5/W and \$1/W, where the first design set corresponds to the lowest power rated converter for scenario 5.

6.5 Result Analysis and Optimized Designs

6.5.1 Ageing scenario analysis

The ageing scenarios consists of weak power mismatches compared to the shading scenarios. The mismatch is also distributed in uniform manner across all the PV cells. Given the 10% standard deviation mismatch in PV cells at 25 years, the power processed in the subMICs would likely be very low. Figure 6.8 and 6.11 from scenario 1 and 2 show that the overall improvement at 20 years is about 2-2.5% for all converter ratings. Comparing the 20 year results in the cost/performance plots in Figure 6.9 and 6.12, the improvements from all the subMIC designs seem similar for each scenario. This is due to the fact that even the lowest power rated converters (10 W) are over 10% of the power of highest 100 W rated substrings. As a result, even the 10 W rated converter are sufficient enough to process most of the mismatched power.

Scenario 2 uses PV cells with double the short circuit current compared to scenario 1.

Both scenarios use the same mismatch distribution in percentage of power. The subMICs in scenario 2 will be processing more power, hence more affected by converter efficiency and power rating. As a result, improvement in scenario 1 is at about 2.5% while scenario 1 shows about 2%.

From the ageing scenario results, we can conclude that the benefits from subMICs are relatively low. This is mainly due to the fact that loss from ageing itself is small. Also, the mismatches are distributed widely over all the PV cells. If we also include the cost of the converters, the SFOM plots show that PV module costs must be higher than \$1/W to justify the cost of even the 10 W design #1. Evaluation was performed on commercially available PV modules. However, if lower power converters can be designed at lower cost and the subMICs are connected to much higher power rated substrings, the benefit of the subMIC would be much better for the ageing scenario. For the all the ageing scenarios, the least costing #1 design would be the most optimal choice.

6.5.2 Shading scenario analysis

Compared to the ageing scenarios, the shading scenarios consists of stronger mismatches. The subMICs in the shading scenarios would be processing more power. Results of scenario 3, 4, and 5 show that subMIC power ratings now dominate the performance improvement. This is shown in Figures 6.14, 6.17, and 6.20. Also, the cost/performance plots in Figure 6.15, 6.18, and 6.21 show a more scattered distribution compared to the ageing cases. Now both cost, power rating and efficiency all contribute to the results. Comparing the distribution with reference to the \$1/W PV module cost justification line, some designs cross under the justification line. Just by analyzing the distribution plots, it is difficult to see which designs are a better optimized for the scenario. The SFOM analysis, as in figure 6.16, 6.19, and 6.22, with a given PV module \$/W cost, gives a better view for comparison.

6.5.3 Optimal designs based on SFOM

Optimal design for a given scenario is selected by choosing the design with the best SFOM. For all the ageing scenarios, #1 design with 10 W rating and 86% efficiency would be optimal. For all the shading scenarios, the best SFOM is found to be design #7 with 25 W rating with 89% efficiency. However, the second best design varies with scenario. Design #9 with 30 W rating and 89% efficiency is the second best for scenario 3 and 5. Design #12 with 35 W rating at 90% efficiency is found to be the second best for scenario 4. The optimal designs and its specifications are shown in Table 6.13.

#	Module rating (W)	Mismatch scenario	Comment	Optimal design	SubMIC $/W with PV module @ $1/W
1	185	Ageing	Reference (ageing)	#1, 10W, η=86%	$0.034
2	318	Ageing	Increased rating (ageing)	#1, 10W, η=86%	$0.020
3	208	Shading 1	Reference (shading)	#7, 25W, η=88%	$0.033
4	297	Shading 1	Increased rating (shading)	#7, 25W, η=88%	$0.023
5	189	Shading 2	Sharp shading pattern	#7, 25W, η=88%	$0.036

Table 6.13: Selected optimized subMIC designs and its specifications.

The scenarios evaluated only included one shading or ageing related mismatch analysis. It does not include both at the same time. If both mismatch scenarios are considered at the same time, performance improvement could be the some of the two scenario results. This would result in better figure of merit.

6.5.4 Design distribution

Optimal subMIC designs were selected based on a defined SFOM analysis over different designs and PV system setup scenarios. Additional analysis is done to understand why the selected designs came out to be optimal. Furthermore, the analysis can reduce the need of full PV simulations.

First, design characteristics are evaluated. SubMIC designs show cost increase with

efficiency and power rating increase. However, the efficiency difference is small and does not have much impact on the system performance. Hence, cost versus power rating comparison as shown in Figure 6.23 can be used to estimate and analyze subMIC performance without the PV simulations.

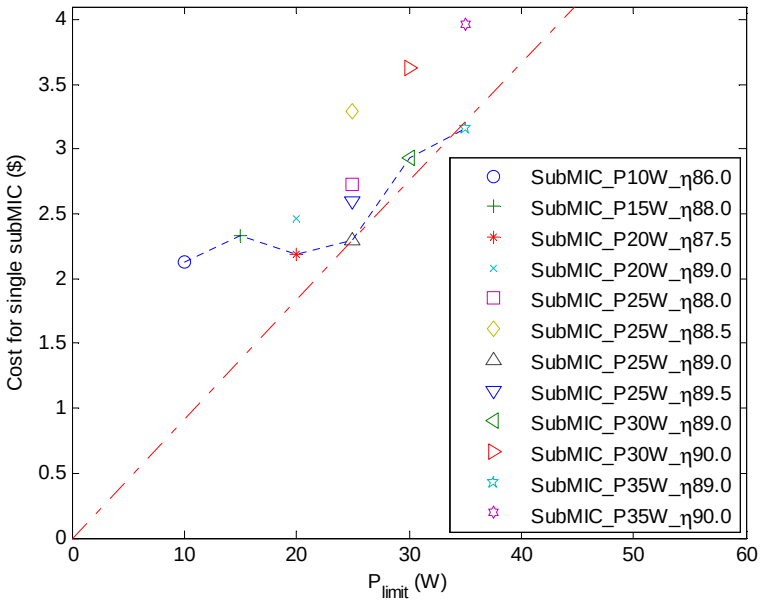


Figure 6.23: Cost versus converter power rating with minimal cost designs shown for each power rating(dotted line) and a reference slope(dot-dash line) to compare other designs to the 25 W minimal cost design.

In Figure 6.23, a contour is drawn over minimal cost designs for a given power rating. The designs close to the contour represents the designs that would be chosen to be the optimal design for any scenario. A reference line is drawn over design #7 from the origin, representing identical $/W for better view.

From the analysis, it has been found that only 6 of the 12 designs need to be evaluated for optimal design selection. Furthermore, the minimal cost contour should monotonically increase, hence design #2 is discarded. As a result, we are left with 5 design candidates for possible optimal designs. Further design set reduction is difficult since the performance improvement to power rating relationship can be highly non-linear. This is shown in Figure

6.24 where the power rating is normalized by the module power for the shading scenarios.

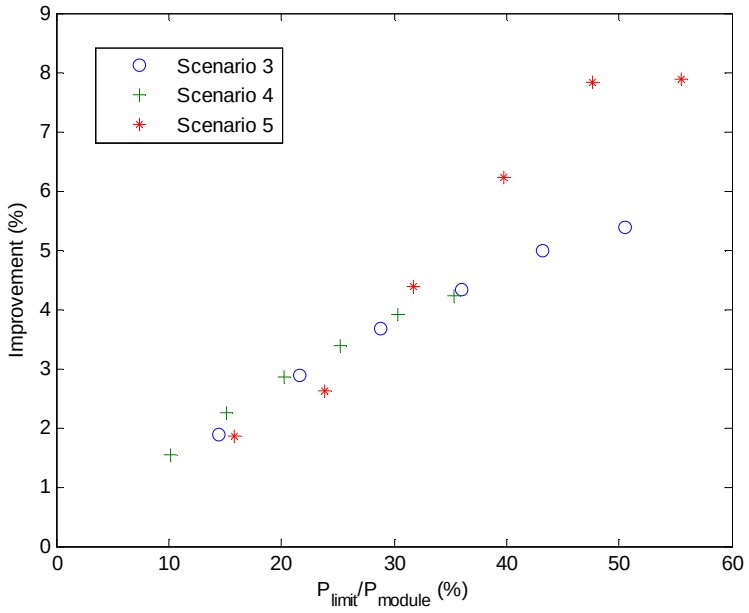


Figure 6.24: Performance improvement versus subMIC power rating to module rating.

In Figure 6.24, benefit of increasing subMIC power rating start to decreases at about 30-50% of the module rating. Scenario 3 and 4 are identical scenarios with different PV module ratings. Hence they show similar characteristics which show a fairly linear relationship between improvement and power rating. It also suggests that the two results scale with the power rating of the PV modules. On the other hand, scenario 5 shows a different pattern where the improvement to power rating slope is non-linear and performance saturates at around 45% of subMIC to module power rating ratio. Scenario 5 is a shading scenario with a stronger and spatially sharper mismatch. This shows that performance improvement ratio is also highly dependent on the shading pattern.

For the ageing scenarios, we also observe that the performance from subMICs are more related to the converter efficiency when converter power ratings are sufficiently high. If we assume all substrings operate at MPP, then we can approximate the PV system power with subMICs as:

$$P_{subMICsystem} \approx P_{ideal} - (1 - \eta_{subMIC}^2) \cdot 0.5 \sum P_{mismatch} \tag{6.8}$$

where the system performance depends on the square of the efficiency times the sum of mismatched power.

Given that converter efficiencies are high, we can furthermore estimate the relative performance improvement to have the following relationship of converter efficiency:

$$\frac{\Delta E}{E_{conv}}(\%, \eta_x) : \frac{\Delta E}{E_{conv}}(\%, \eta_y) \approx \eta_x^2 : \eta_y^2 \tag{6.9}$$

Figures 6.25 and 6.26 show how the estimations match the simulation results.

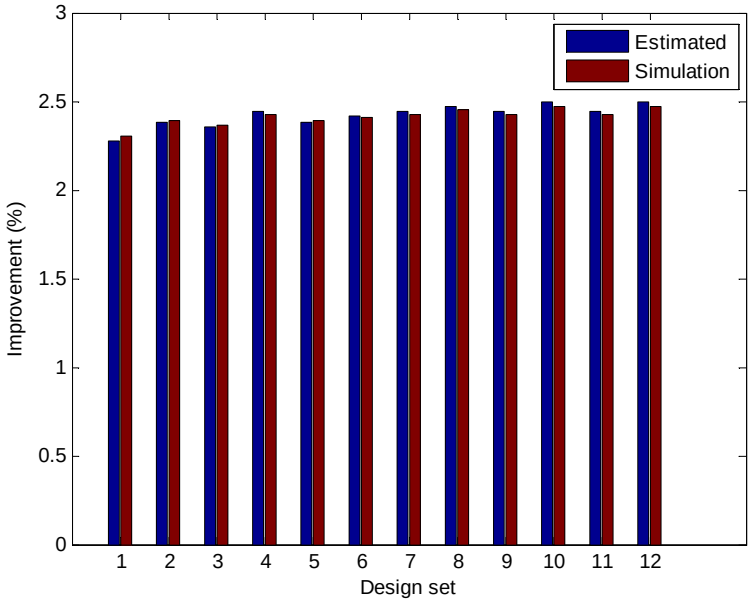


Figure 6.25: Comparison of estimated and simulated system performance improvements for scenario 1.

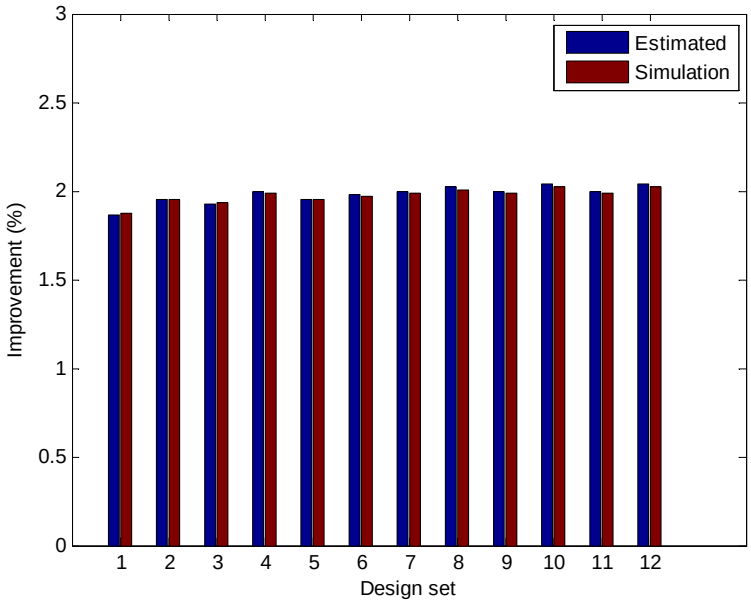


Figure 6.26: Comparison of estimated and simulated system performance improvements for scenario 2.

Results show that a single simulation with a particular design set can be sufficient to estimate the results for other sets of design.

Analysis shows that performance of the subMICs can be estimated between the results of the same shading scenario with different PV power ratings. However, if different shading scenarios are used, it would be difficult to estimate performance without evaluation through simulation. For a performance saturation case as in the ageing mismatch scenario, efficiency can be used to determine the relative performance from a single simulation result.

Chapter 7

Conclusions

This dissertation presents design and optimization of sub-module integrated converters (subMICs) in the isolated-port differential power processing (DPP) photovoltaic (PV) system architecture. Due to the series connection of PV cells, conventional PV systems based on string-level or system-level power electronics are prone to significant performance degradation related to mismatches among the PV cells caused by partial shading, temperature gradients, and tolerances in cell parameters [10,11]. Distributed power processing using high-efficiency switched-mode power power converters at the PV module or sub-module level can be used to mitigate such performance degradation [1,17–20]. Improving the energy-capture performance of a PV system while minimizing the cost overhead associated with power converters is a challenge. PV system installations are not all alike, ranging from relatively small rooftop residential systems to large commercial or utility-scale systems. In particular, residential systems are very often subject to varying partial shading conditions caused by nearby trees or roof features [48]. In commercial or utility-scale systems, mismatch conditions are present due to tolerances parameters (which tend to grow as the system ages), temperature gradients, and inter-row shading [49]. Performance of distributed power electronics architecture in general, and DPP architectures in particular, depend on the system mismatch scenario. Hence, it is desirable to have the converter designs optimized for each setup to maximize performance improvements while reducing cost. In the isolated-port DPP architecture [1],

which is the focus of this thesis, optimizing the subMIC design requires understanding of the DPP architecture, converter design and control issues, as well as the PV system installation environment.

An advantage of the DPP architecture is that the DPP subMICs can provide for power matching among mismatched PV substrings, while processing only a fraction of the full PV power. This allows the use of low power rated subMICs, while the performance of the system is not critically sacrificed. Also, the converter efficiency does not critically impact the system energy-capture performance, in contrast to full power processing architectures such as DC optimizers [13, 14], where the converter efficiency is simply a multiplicative factor in the overall system efficiency. The relatively low power rating of the subMICs means that they can be designed at a lower cost, allowing subMICs to be favorably deployed at a finer granularity compared to full power processing architectures. Importantly, in the DPP architecture, there are no insertion losses under no-mismatch conditions. Hence, the system efficiency can be very close to 100% in cases when mismatches are negligible.

The subMICs in the isolated-port DPP architecture can be controlled using a simple voltage balancing scheme without the need for current sensing or a central controller [2, 3]. The control approach is simple, which is another reason the system performance can be improved, while the cost and size of the subMICs are kept to a minimum. Under mismatch conditions, the system with subMICs in the isolated-port DPP architecture maintains near-constant maximum power point (MPP) voltage. This is not only convenient for maximum power point tracking (MPPT) at the PV string or system level, but can bring in additional performance benefits when subMICs are applied at the submodule-level in combination with a module-level micro-inverter. With embedded subMICs, a micro-inverter can be designed to effectively capture module power over a narrow MPP voltage range, with improved efficiency.

The thesis presents details of subMIC converter and controller designs, emphasizing the impact of subMIC design on system energy-capture performance and cost. In Chapter 3, a prototype board is described with 3 subMICs serving as bypass diode replacements, to fit

inside the junction box of a commercial PV module. The subMICs include custom designed CMOS controllers, which effectively perform voltage balancing and protection functions, while demonstrating simplicity and low-cost potentials. The subMIC controller IC is designed to maintain high converter efficiency at low load, while keeping the converters in their safe operating range. The design also ensures that the control circuitry does not contribute to any significant insertion losses under no mismatch operating conditions.

In Chapter 5, energy-capture performance of the prototype system is evaluated under various conditions using 90% efficient subMICs rated at one third of the PV substring power rating. Both indoor and outdoor experiments confirm that the designed system outperforms the conventional system in terms of energy capture and system efficiency. The outdoor experiments with the subMIC-enhanced PV module show over 98% system efficiency under up to 30% shading mismatch. The performance improvement over the conventional PV module with bypass diodes is 12.8% at 30% mismatch. Performance improvement at 60% mismatch is shown to be over 25%.

A system cost/performance analysis is presented in Chapter 6 of this thesis. Energy capture performance is analyzed using the PVsims cell-level simulation tool [44, 45] under realistic solar irradiation data, in several representative system scenarios corresponding to different mismatch conditions. System energy capture performances depend on the subMIC power rating and efficiency. SubMIC cost model is developed using realistic volume pricing of converter components including semiconductors, magnetics, and printed circuit board. The cost is evaluated for several power ratings and for several different design options to evaluate how the subMIC cost depends on power rating and efficiency. A performance/cost figure of merit is introduced to select the optimum design for a given installation scenario. The best figure of merit for all the shading scenario evaluated was found to be a \$0.02/W design with 25 W rating and 88% efficiency. Optimized designs show performance improvements of 3.5-4.5% in residential setups with tree shading, and 6.5% in a pole shading scenario in a commercial PV system.

In summary, the main contributions of this thesis, which is focused on design, implementation and evaluation of submodule integrated converters in the isolated-port different power processing PV architecture, are as follows:

- The subMIC control methods are developed and implemented on a custom CMOS integrated circuit. The subMIC CMOS controller demonstrates simple voltage-balancing control, power limiting, and protection features. It replaces numerous discrete and passive components, reducing the subMIC size, and showing potentials for low-cost realization. The controller power consumption is minimized.

- Using the subMIC controllers, subMIC power converters capable of processing up to 60 W each are design based on the bi-directional flyback configuration using optimized planar magnetics. Three such subMICs are assembled on a board that fits easily into the junction box of a commercial 175 W PV module. The subMICs are 90% efficient over a wide range of power levels, with less than 100 mW quiescent power consumption, thus minimizing system losses under no-mismatch conditions.

- Performance of the subMIC-enhanced PV module is demonstrated and verified in laboratory and in outdoor tests, included performance tests with power-limited subMICs. The module-level efficiency is found to be greater than 99.4% at up to 25% mismatch, and greater than 98.3% at up to 50% mismatch. The outdoor experiments with the subMIC-enhanced PV module show over 98% system efficiency under up to 30% shading mismatch. The performance improvement over the conventional PV module with bypass diodes is 12.8% at 30% mismatch. Performance improvement at 60% mismatch is shown to be over 25%.

- A system cost/performance analysis is performed. A performance/cost figure of merit is introduced to select the optimum design for a given installation scenario. A \$0.02/W design with 25 W rating and 88% efficiency is found to be optimal. It

shows 3.5-6.5% energy-capture performance improvements in various relevant shading scenarios.

7.1 Future Work

The subMIC controller can be improved further, as proposed in the thesis. A minimal cost and size design can be achieved using the new design, resulting in better performance versus cost ratios. Also, a de-energizing feature can be easily added to the subMICs to limit the open-circuit voltage V_{OC} of a module to be closer to V_{MPP}. This feature would allow more PV modules to be connected to a PV inverter of the same voltage rating and would also simplify compliance with safety regulations.

The experimental system evaluations, limited to a module level in this thesis, can be expanded to larger PV installations.

The work done in the dissertation was limited to a DPP subMIC system using bi-directional flybacks at the substring level. Future work can be extended to subMIC designs at a finer granularity level to increase energy-capture performance improvements further and potentially open opportunities for higher level of integration in subMIC realizations. There are potentials that such subMICs could be designed at much lower power and lower cost per Watt. Based on the approaches presented in this thesis, further detailed performance evaluations, in combination with cost analyses of alternative subMIC designs and realizations, can be performed to determine the optimal level of granularity of subMICs in the isolated-port DPP architecture.

The combination of DPP subMICs embedded within a module-level micro-inverter deserves further attention. Micro-inverters perform MPPT at the module level. Some micro-inverters shut off when the MPP voltage deviates significantly. The DPP subMICs can not only improve energy capture because of the effectively finer-granularity MPPT, but can also improve the energy capture and efficiency by maintaining the module-level MPP voltage in

a much narrower range, with a single maximum.

The overall design and system optimization can be extended further. First, different figure of merits can be considered. The figure of merit presented in Chapter 6 only considers the PV module cost to evaluate the cost effectiveness of the subMIC. However, PV modules are only a portion of the PV system cost. Other balance of system (BOS) and installation costs can be included in the cost/performance evaluation. Ultimately, minimizing the levelized cost of electricity (LCOE) can be used as an overarching optimization goal.

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Appendix A

Circuit Level Design of the SubMIC Controller

This chapter lists the circuit level design of the blocks that form the subMIC controller IC.

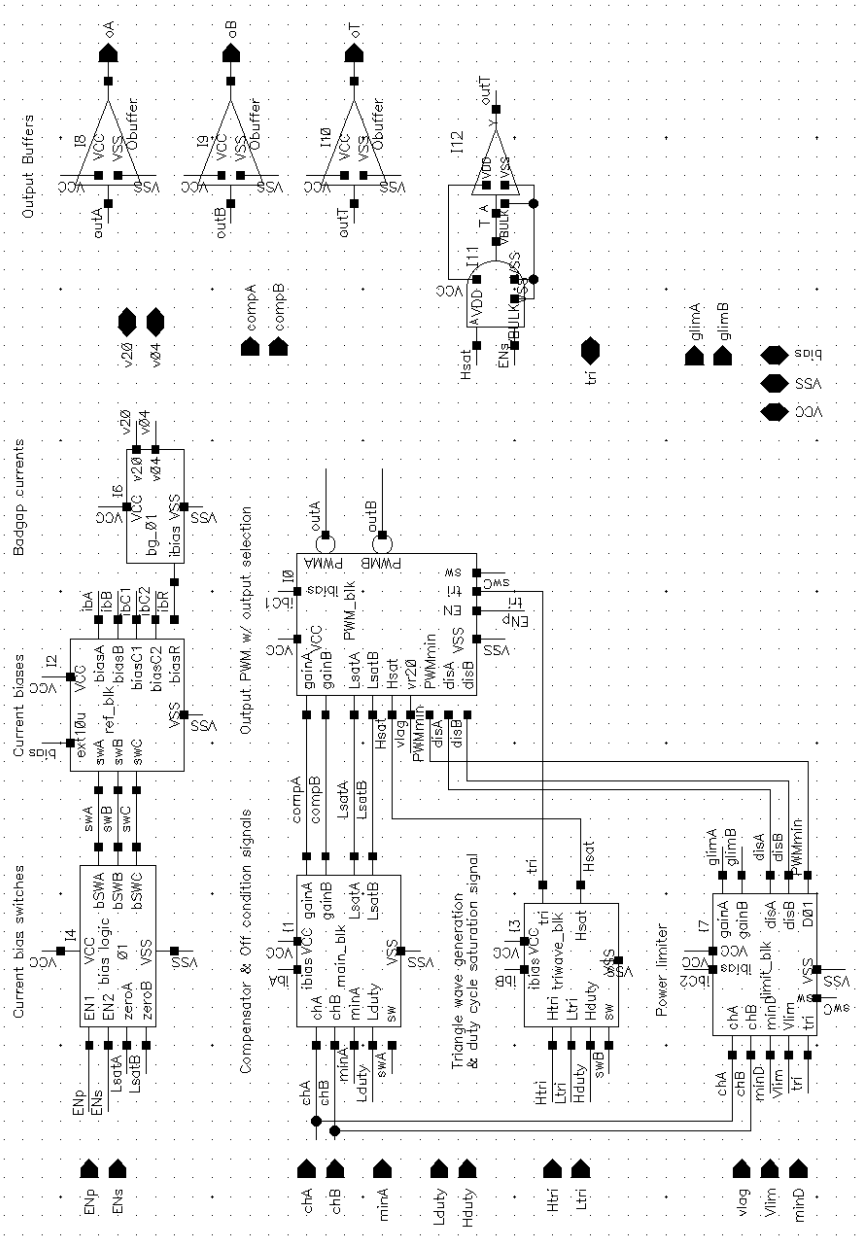

Figure A.1: SubMIC schematic.

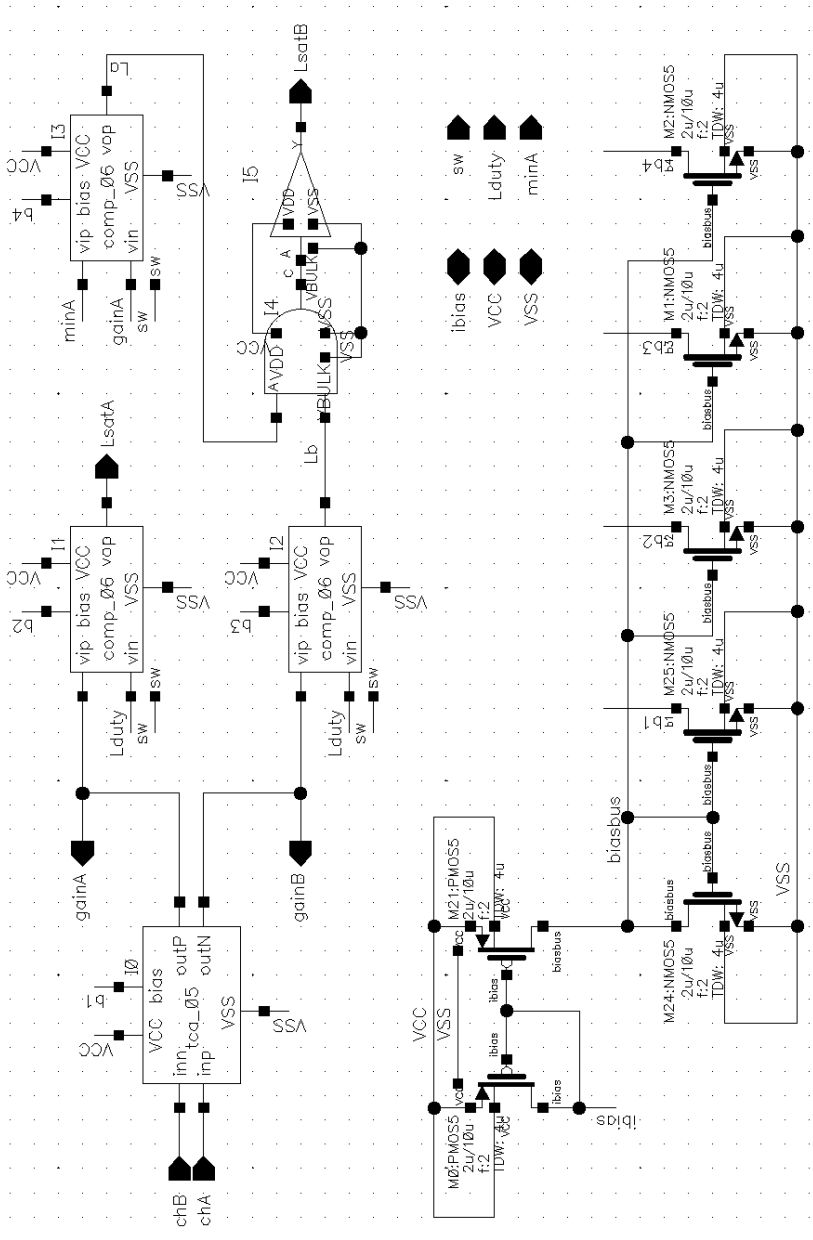

Figure A.2: *blks_main* schematic.

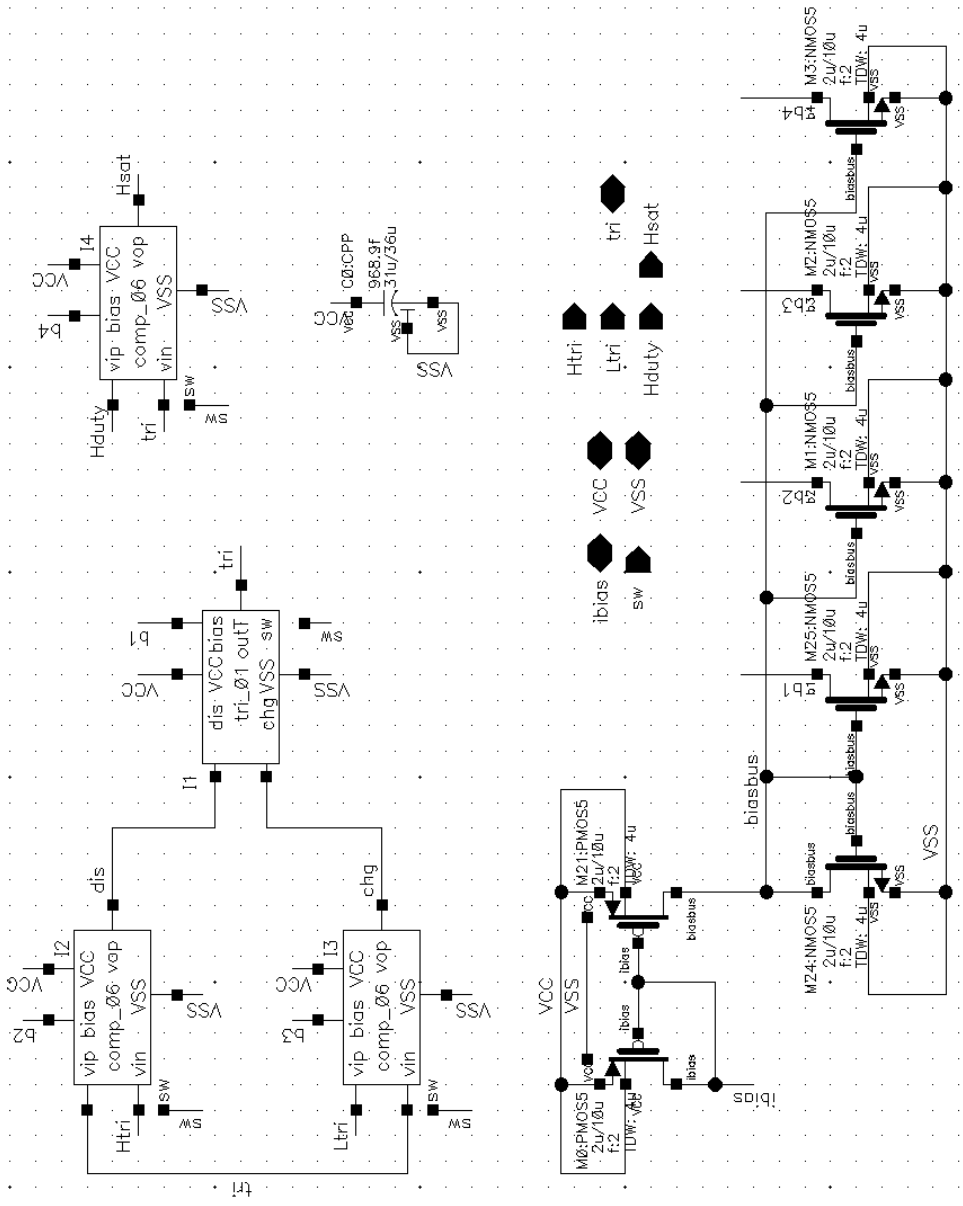

Figure A.3: *blks_triwave* schematic.

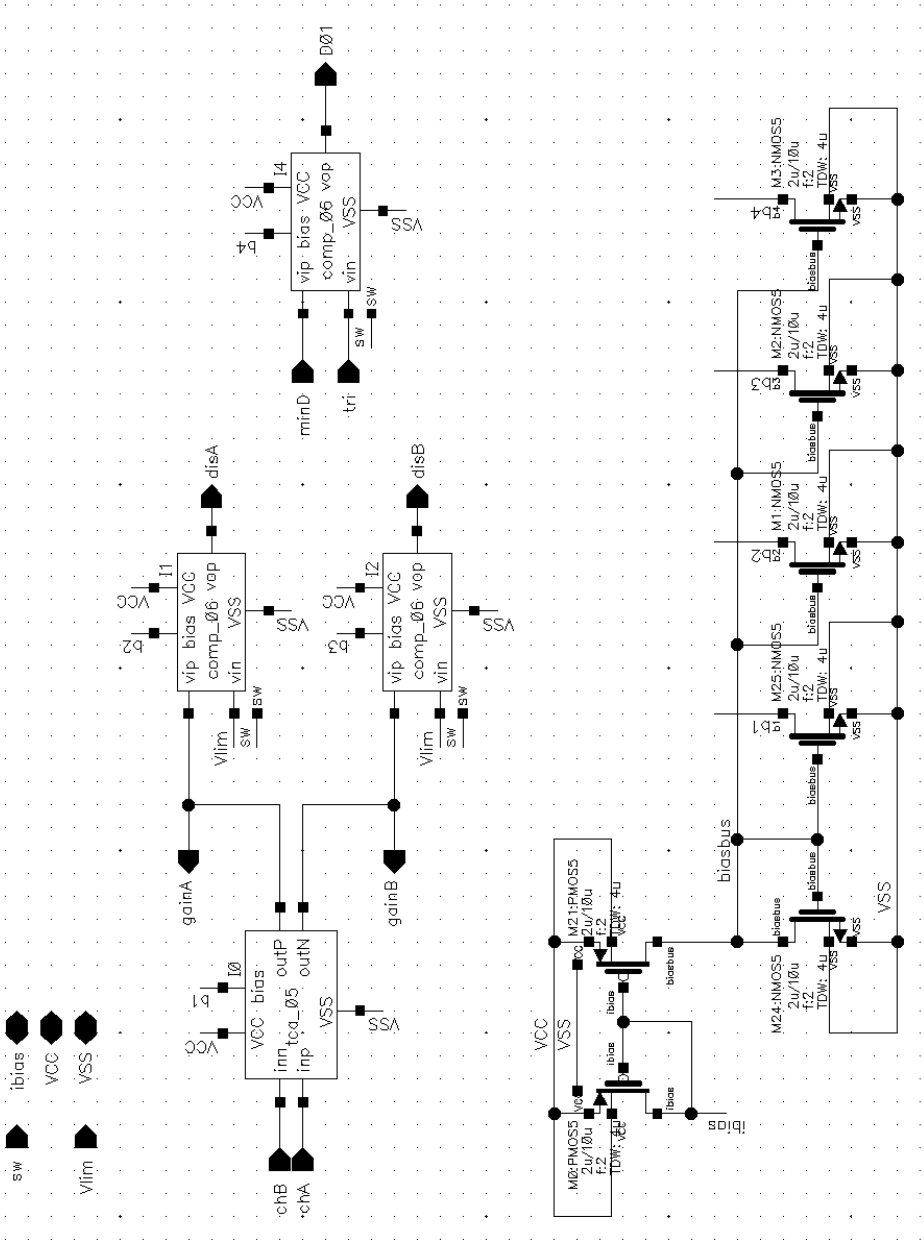

Figure A.4: *blks_limit* schematic.

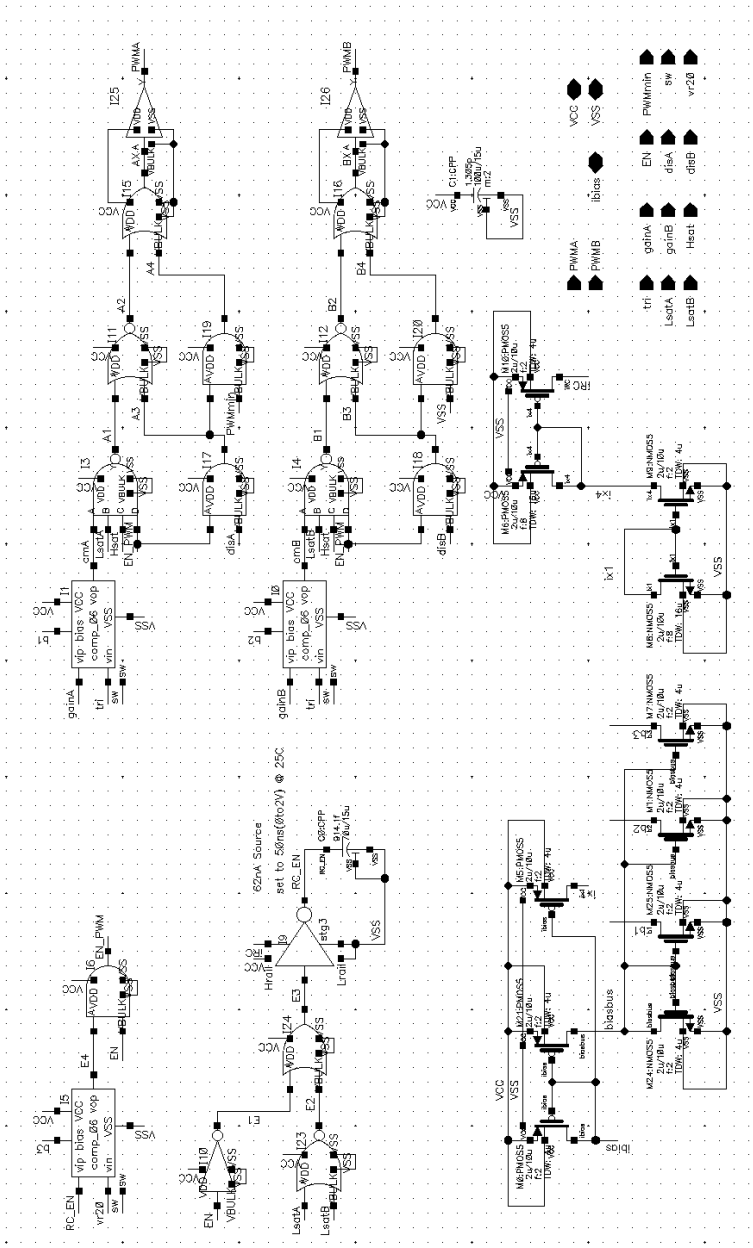

Figure A.5: *blks_PWM* schematic.

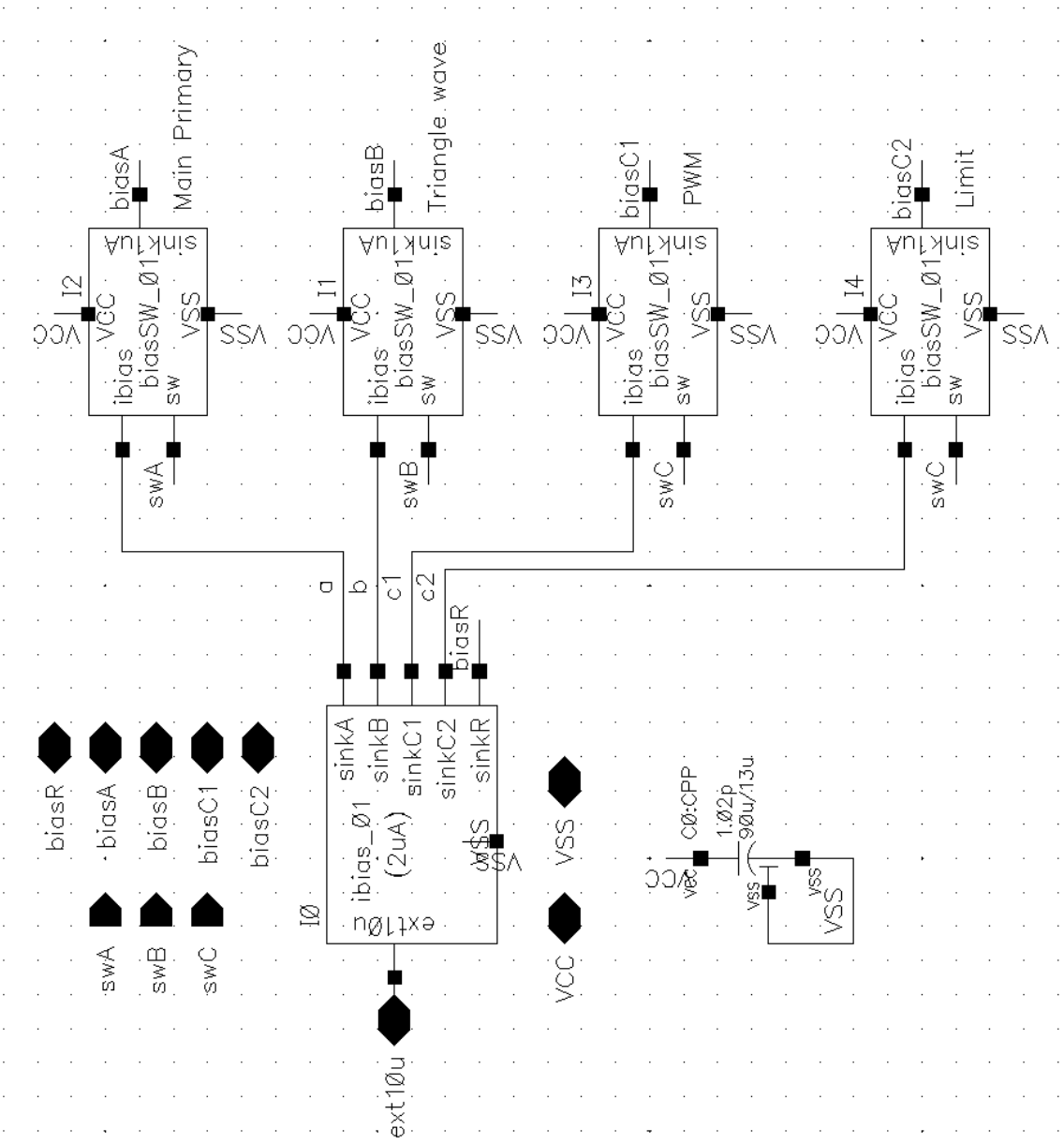

Figure A.6: *blks_ref* schematic.

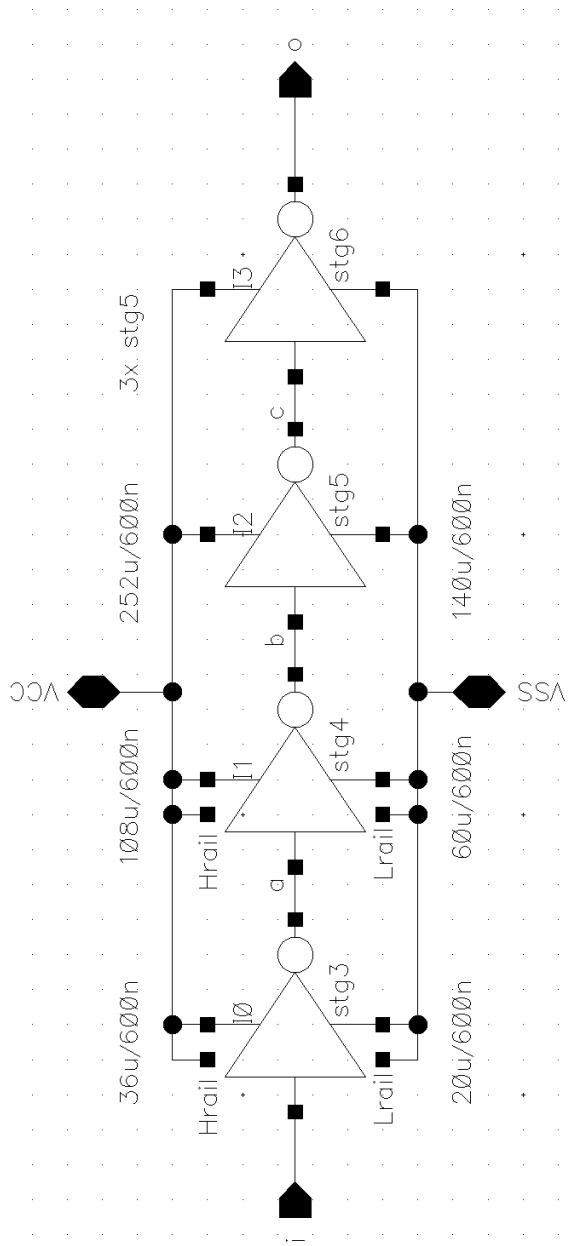

Figure A.7: *blks_oBuffer* schematic.

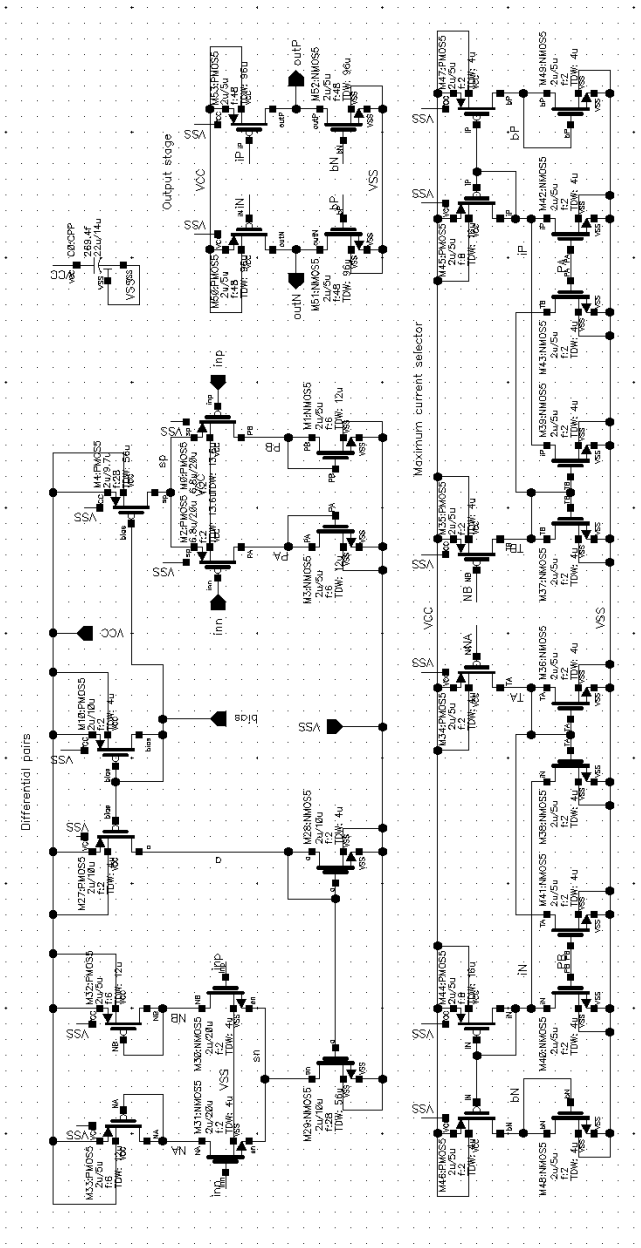

Figure A.8: *mdl_tca* schematic.

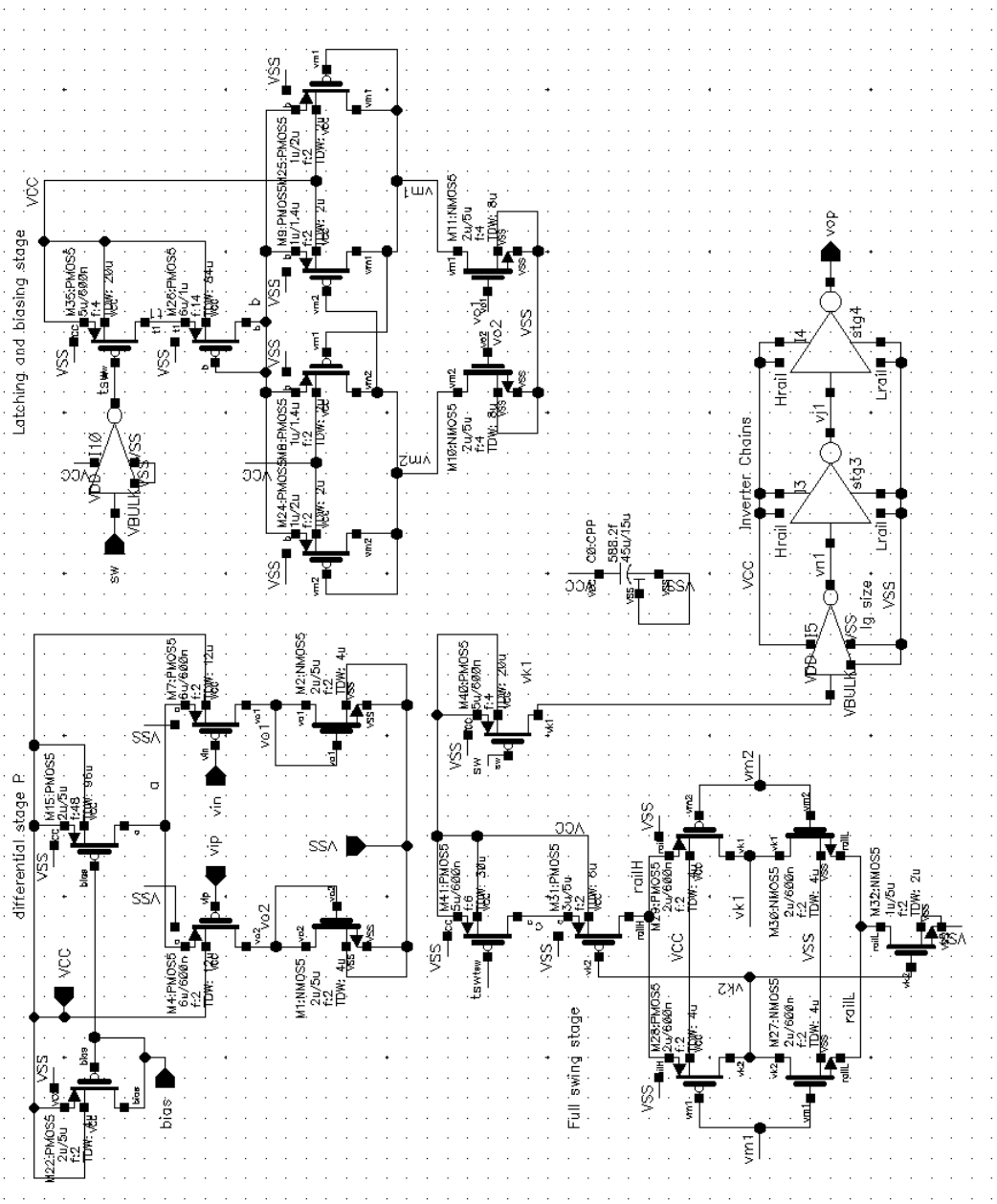

Figure A.9: *mdl_comp* schematic.

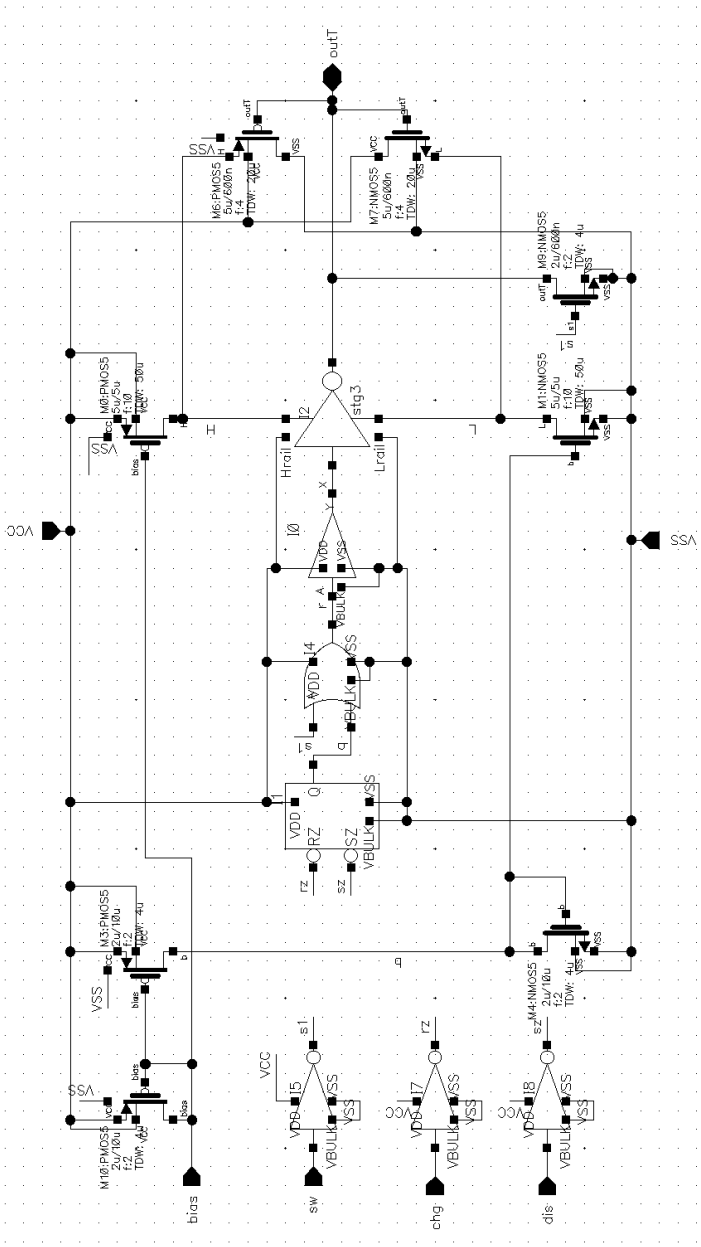

Figure A.10: *mdl_tri* schematic.

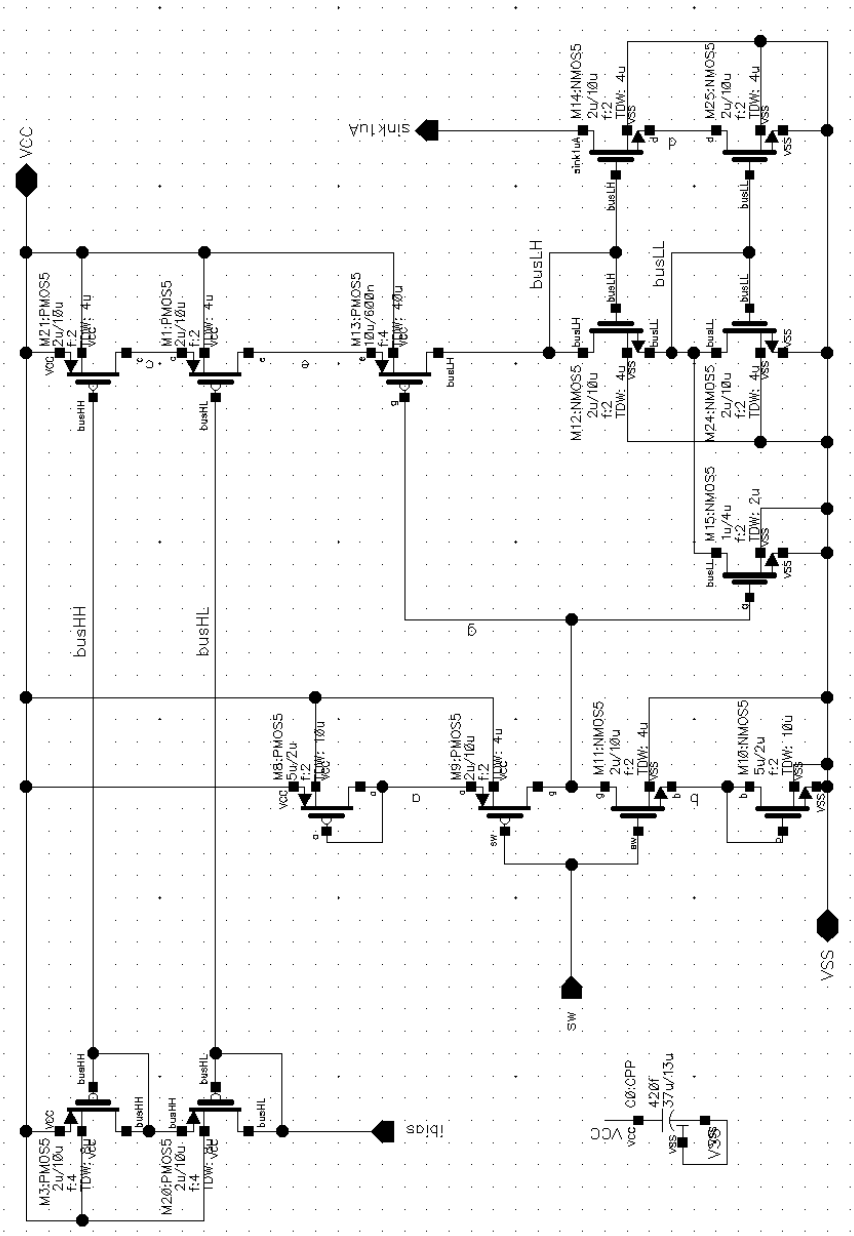

Figure A.11: *mdl_biasSW* schematic.

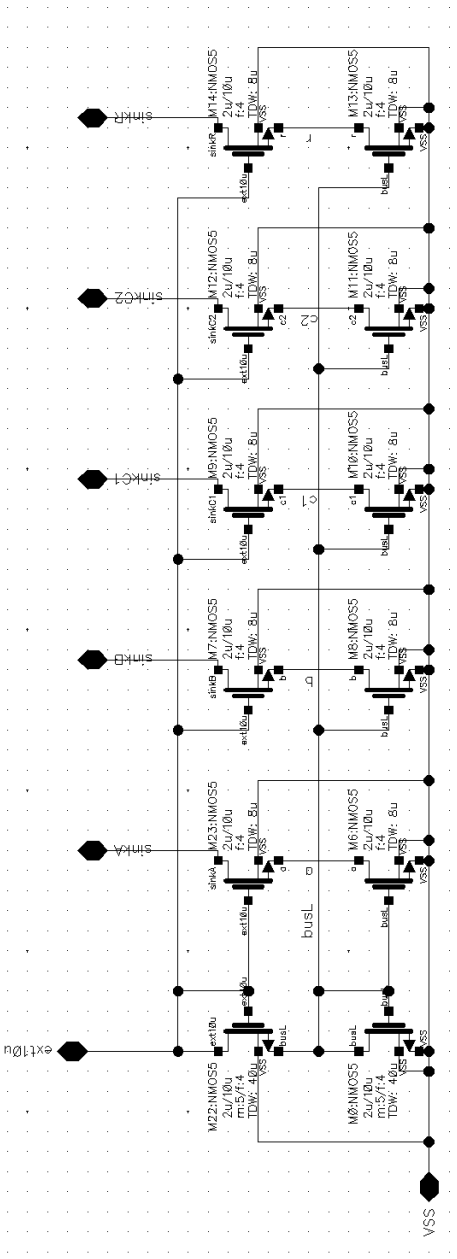

Figure A.12: *mdl_ibias* schematic.

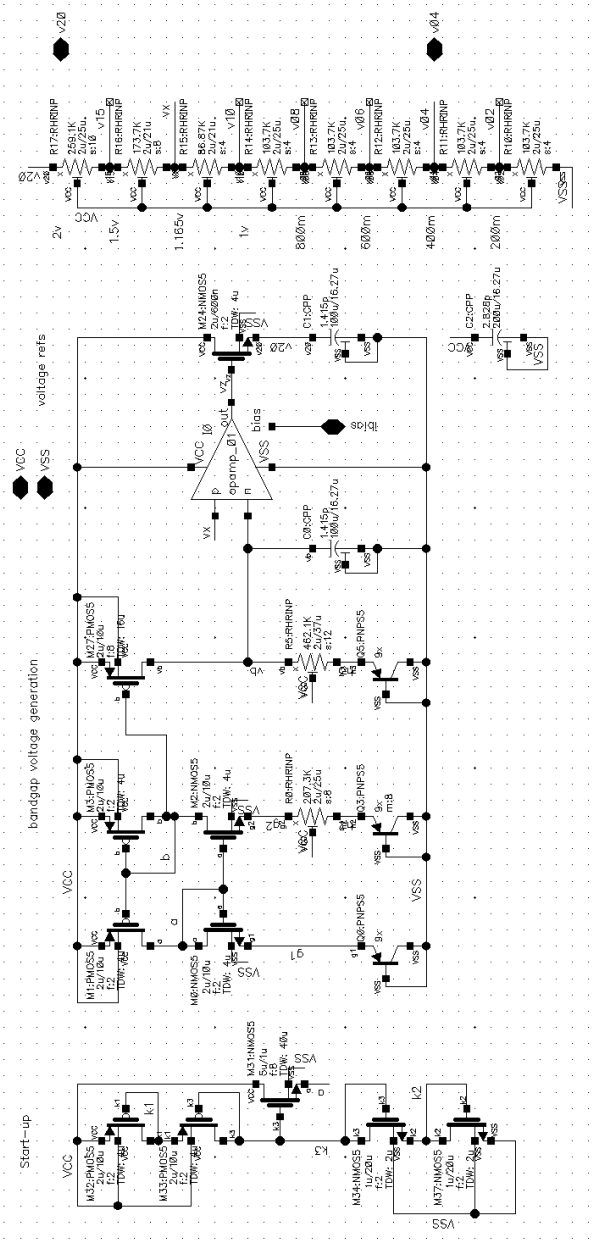

Figure A.13: *mdl_bg* schematic.

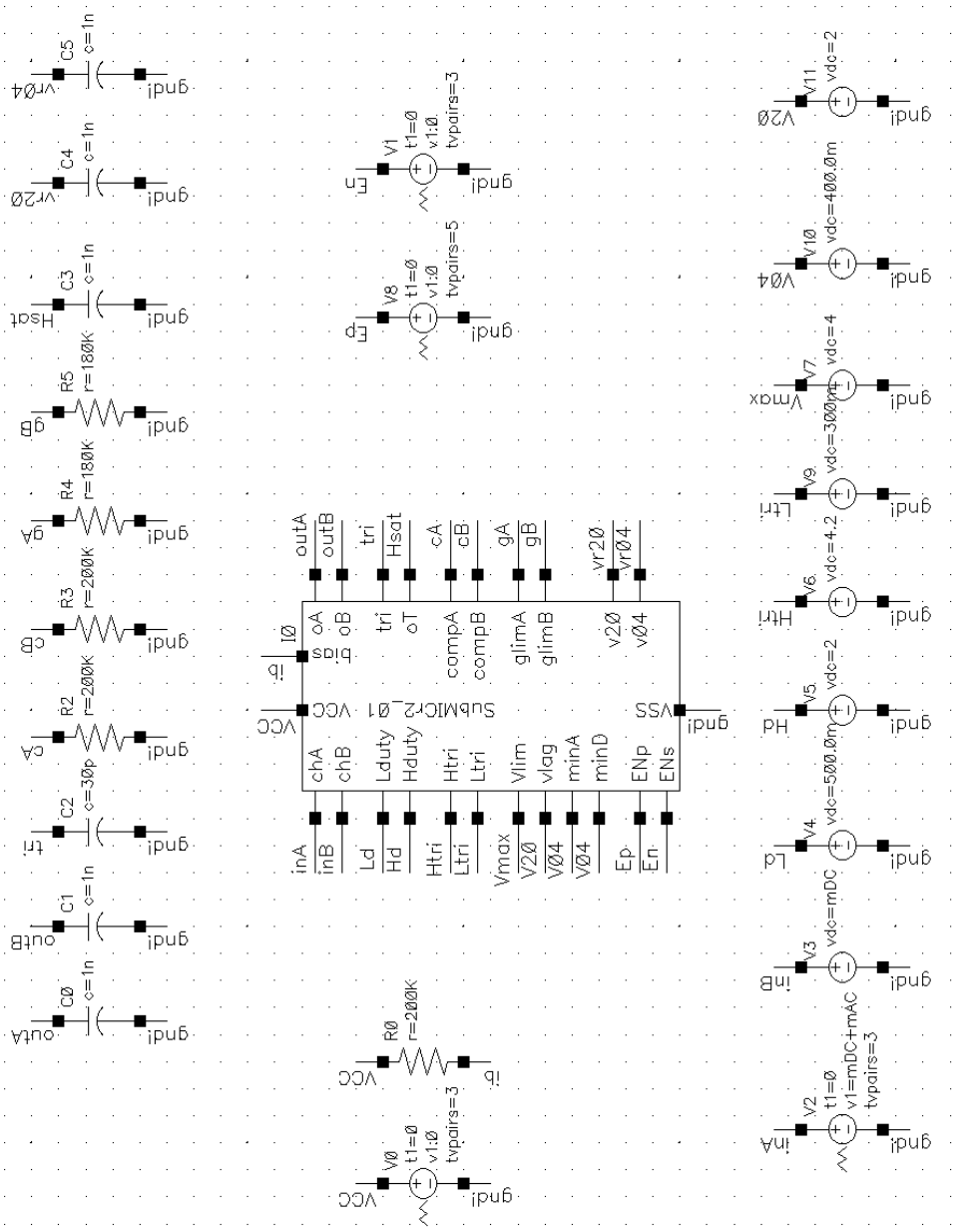

Figure A.14: SubMIC test setup schematic.